

Failure Modes, Effects and Diagnostic Analysis

Project:
BCO CL2 / CL4 / ML2 surge arrester series

Customer:

DEHN SE
Neumarkt
Germany

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Management summary

This report summarizes the results of the hardware assessment carried out on the BCO CL2 / CL4 / ML2 surge arrester series in the versions listed in the drawings referenced in section 2.4.1. Table 1 gives an overview of the different configurations that belong to the considered BCO CL2 / CL4 / ML2 surge arrester series.

The hardware assessment consists of a Failure Modes, Effects and Diagnostics Analysis (FMEDA). A FMEDA is one of the steps taken to achieve functional safety assessment of a device per IEC 61508. From the FMEDA, failure rates are determined and consequently the Safe Failure Fraction (SFF) is calculated for the device. For full assessment purposes all requirements of IEC 61508 must be considered.

Table 1: Configuration overview BCO CL2 / CL4 / ML2 surge arrester series

CL2	
BCO CL2 BE 12 BCO CL2 BE 24 BCO CL2 BE 48	Compact combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting two single lines sharing a common reference potential as well as unbalanced interfaces.
BCO CL2 BD 12 BCO CL2 BD 24 BCO CL2 BD 48	Compact combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of unearthed balanced interfaces.
BCO CL2 BE HF 5	Compact combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting two single lines of high-frequency transmissions sharing a common reference potential as well as unbalanced interfaces.
BCO CL2 BD HF 5	Compact combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of unearthed high-frequency bus systems as well as balanced interfaces.
BCO CL2 BD EX 24	Compact combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of intrinsically safe measuring circuits and bus systems, meets FISCO requirements. Insulation strength > 500 V line-ground.
BCO CL2 BD HC10A 24	Space-saving, compact combined arrester with a width of 12 mm and push-in connection technology with status indication for protecting one pair in unearthed DC supplies for IT systems and measuring and control circuits. Two-pole arrester for protecting DC supplies of up to 10 A nominal current.
BCO CL2 B 180	Compact lightning current arrester with a width of 6 mm and status indication with push-in connection technology for protecting two single lines for lightning.
BCO CL2 E 12 BCO CL2 E 24 BCO CL2 E 48	Compact surge arrester with a width of 6 mm and status indication with push-in connection technology. Finely limiting, single-stage surge protection with powerful diodes for protecting two single cores sharing a common reference potential as well as unbalanced interfaces.

CL4	
BCO CL4 BC 24	Compact combined lightning current and surge arrester with a width of 12 mm and status indication with push-in connection technology for protecting of unearthed 4-conductor measurement circuits for IT systems and measuring and control circuits.
ML2	
BCO ML2 BE 12 BCO ML2 BE 24 BCO ML2 BE 48 BCO ML2 BE 180	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting two single lines sharing a common reference potential as well as unbalanced interfaces. With signal disconnection for maintenance purposes.
BCO ML2 BD 12 BCO ML2 BD 24 BCO ML2 BD 48 BCO ML2 BD 180	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of unearthed balanced interfaces. With signal disconnection for maintenance purposes.
BCO ML2 BE HF 5 BCO ML2 BE HF 24	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting two single lines of high-frequency transmissions sharing a common reference potential as well as unbalanced interfaces. With signal disconnection for maintenance purposes.
BCO ML2 BD HF 5 BCO ML2 BD HF 24	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of unearthed high-frequency bus systems as well as balanced interfaces. With signal disconnection for maintenance purposes.
BCO ML2 BD EX 24	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of intrinsically safe measuring circuits and bus systems, meets FISCO requirements. Insulation strength > 500 V line-ground. With signal disconnection for maintenance purposes.
BCO ML2 BD HC5A 24	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of unearthed balanced interfaces with high nominal current for IT systems and measuring and control circuits. With signal disconnection for maintenance purposes.
BCO ML2 B 180	Modular lightning current arrester with a width of 6 mm and status indication with push-in connection technology for protecting two single lines for lightning
BCO ML2 MVG 230	Space-saving, modular surge arrester with a width of 6 mm and push-in connection technology with status indication for protecting 2 lines of stranded unearthed signal interfaces with a nominal voltage of 230 V.
BCO ML2 BPD 24	Modular combined lightning current and surge arrester with a width of 6 mm and status indication with push-in connection technology for protecting one pair of unearthed balanced interfaces in 24 V DC systems. Integrated PTC resistors allow to reliably reset the arrester after the system circuit has been affected by short-circuit currents up to 40 A. With signal disconnection for maintenance purposes.

For safety applications only the described configurations were considered. All other possible variants or electronics are not covered by this report.

Surge protective devices are not considered to be elements according to IEC 61508-4 section 3.4.5 as they are not performing one or more element safety functions. Therefore, there is no need to calculate a SFF (Safe Failure Fraction). Only the interference on a safety functions needs to be considered. This interference is expressed in a contribution to the overall PFD_{AVG} / PFH.

The failure rates used in this analysis are from the *exida* Electrical & Mechanical Component Reliability Handbook for Profile 1.

The following tables show how the above stated requirements are fulfilled under worst-case assumptions.

Table 2: Failure rates [1] BCO *L2 BE 12, BCO *L2 BE 24, BCO *L2 BE 48, BCO ML2 BE 180

	exida Profile 1	
	Analysis 1 [2]	Analysis 2 [3]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**7**
Fail Dangerous Undetected (λ_{DU})	**10**	**3**
Total failure rate	**13 FIT**	**13 FIT**

Table 3: Failure rates [1] BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48, BCO ML2 BD 180

	exida Profile 1	
	Analysis 1 [2]	Analysis 2 [3]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**2**
Fail Dangerous Undetected (λ_{DU})	**10**	**8**
Total failure rate	**13 FIT**	**13 FIT**

[1] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[2] Analysis 1 represents a worst-case analysis.

[3] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 4: Failure rates [4] BCO *L2 BE HF 5, BCO ML2 BE HF 24

	exida Profile 1	
	Analysis 1 [5]	Analysis 2 [6]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**17**
Fail Dangerous Undetected (λ_{DU})	**20**	**3**
Total failure rate	**23 FIT**	**23 FIT**

Table 5: Failure rates [4] BCO *L2 BD HF 5, BCO ML2 BD HF 24

	exida Profile 1	
	Analysis 1 [5]	Analysis 2 [6]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**13**
Fail Dangerous Undetected (λ_{DU})	**16**	**3**
Total failure rate	**19 FIT**	**19 FIT**

[4] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[5] Analysis 1 represents a worst-case analysis.

[6] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 6: Failure rates [7] BCO *L2 BD EX 24

	exida Profile 1	
	Analysis 1 [8]	Analysis 2 [9]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**6**
Fail Dangerous Undetected (λ_{DU})	**10**	**4**
Total failure rate	**13 FIT**	**13 FIT**

Table 7: Failure rates [7] BCO *L2 B 180

	exida Profile 1	
	Analysis 1 [8]	Analysis 2 [9]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**2**
Fail Dangerous Undetected (λ_{DU})	**4**	**2**
Total failure rate	**6 FIT**	**6 FIT**

[7] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[8] Analysis 1 represents a worst-case analysis.

[9] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 8: Failure rates [10] BCO ML2 MVG 230

	exida Profile 1	
	Analysis 1 [11]	Analysis 2 [12]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**6**	**2**
Total failure rate	**8 FIT**	**8 FIT**

Table 9: Failure rates [10] BCO ML2 BPD 24

	exida Profile 1	
	Analysis 1 [11]	Analysis 2 [12]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**8**	**8**
Fail Dangerous Detected (λ_{DD})	**0**	**2**
Fail Dangerous Undetected (λ_{DU})	**11**	**9**
Total failure rate	**19 FIT**	**19 FIT**

[10] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[11] Analysis 1 represents a worst-case analysis.

[12] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 10: Failure rates [13] BCO CL2 BD HC10A 24

	exida Profile 1	
	Analysis 1 [14]	Analysis 2 [15]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**8**
Fail Dangerous Undetected (λ_{DU})	**12**	**4**
Total failure rate	**14 FIT**	**14 FIT**

Table 11: Failure rates [13] BCO CL2 E 12 / 24 / 48

	exida Profile 1	
	Analysis 1 [14]	Analysis 2 [15]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**5**
Fail Dangerous Undetected (λ_{DU})	**6**	**1**
Total failure rate	**8 FIT**	**8 FIT**

[13] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[14] Analysis 1 represents a worst-case analysis.

[15] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 12: Failure rates [16] BCO CL4 BC 24

	exida Profile 1	
	Analysis 1 [17]	Analysis 2 [18]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**10**
Fail Dangerous Undetected (λ_{DU})	**13**	**3**
Total failure rate	**16 FIT**	**16 FIT**

Table 13: Failure rates [16] BCO ML2 BD HC5A 24

	exida Profile 1	
	Analysis 1 [17]	Analysis 2 [18]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**5**
Fail Dangerous Undetected (λ_{DU})	**7**	**2**
Total failure rate	**9 FIT**	**9 FIT**

The failure rates are valid for the useful life of the BCO CL2 / CL4 / ML2 surge arrester series (see Appendix 2).

[16] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[17] Analysis 1 represents a worst-case analysis.

[18] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

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1 Purpose and Scope

This document shall describe the results of hardware assessment according to IEC 61508 carried out on the BCO CL2 / CL4 / ML2 surge arrester series in the versions listed in the drawings referenced in section 2.4.1. Table 1 gives an overview of the different configurations that belong to the considered BCO CL2 / CL4 / ML2 surge arrester series.

The FMEDA builds the basis for an evaluation whether a sensor or final element subsystem, including the BCO CL2 / CL4 / ML2 surge arrester series meets the average Probability of Failure on Demand (PFD_{AVG}) / Probability of dangerous Failure per Hour (PFH) requirements and if applicable the architectural constraints / minimum hardware fault tolerance requirements per IEC 61508 / IEC 61511. It **does not** consider any calculations necessary for proving intrinsic safety or the correct functioning of the surge protective devices.

2 Project management

2.1 *exida*

exida is one of the world's leading accredited Certification Bodies and knowledge companies specializing in automation system safety, availability, and cybersecurity with over 500-person years of cumulative experience in functional safety, alarm management, and cybersecurity. Founded by several of the world's top reliability and safety experts from manufacturers, operators and assessment organizations, *exida* is a global corporation with offices around the world. *exida* offers training, coaching, project-oriented consulting services, safety engineering tools, detailed product assurance and ANSI accredited functional safety and cybersecurity certification. *exida* maintains a comprehensive failure rate and failure mode database on electronic and mechanical equipment and a comprehensive database on solutions to meet safety standards such as IEC 61508.

2.2 Roles of the parties involved

DEHN SE	Manufacturer of the BCO CL2 / CL4 / ML2 surge arrester series.
Exida	Performed the hardware assessment.

DEHN SE contracted *exida* in May 2024 with the FMEDAs for the new types BCO CL2 E 12 / 34 / 48, BCO CL4 BC 24 and BCO ML2 BD HC5A 24.

2.3 Standards / Literature used

The services delivered by *exida* were performed based on the following standards / literature.

[N1]	IEC 61508-2:2010	Functional Safety of Electrical/Electronic/Programmable Electronic Safety-Related Systems
[N2]	Electrical Component Reliability Handbook, 5th Edition, 2021	*exida* LLC, Electrical & Mechanical Component Reliability Handbook, 5th Edition, 2021 Vol. 1 – Electrical Components ISBN 978-1-934977-09-5

2.4 Reference documents

2.4.1 Documentation provided by the customer

[D1]	Schaltbild_Stückliste_BCO CL2 BD 12.pdf	Circuit diagram / parts list "BCO CL2 BD 12" of 07.11.19
[D2]	Schaltbild_Stückliste_BCO CL2 BD 24.pdf	Circuit diagram / parts list "BCO CL2 BD 24" of 07.11.19
[D3]	Schaltbild_Stückliste_BCO CL2 BD 48.pdf	Circuit diagram / parts list "BCO CL2 BD 48" of 07.11.19
[D4]	Schaltbild_Stückliste_BCO CL2 BD EX 24.pdf	Circuit diagram / parts list "BCO CL2 BD EX 24" of 07.11.19
[D5]	Schaltbild_Stückliste_BCO CL2 BD HF 5.pdf	Circuit diagram / parts list "BCO CL2 BD HF 5" of 23.04.19

[D6]	Schaltbild_Stückliste_BCO CL2 BE HF 5.pdf	Circuit diagram / parts list “BCO CL2 BE HF 5” of 23.04.19
[D7]	Schaltbild_Stückliste_BCO CL2 B 180.pdf	Circuit diagram / parts list “BCO CL2 B 180” of 23.04.19
[D8]	Schaltbild_Stückliste_BCO CL2 BE 12.pdf	Circuit diagram / parts list “BCO CL2 BE 12” of 23.04.19
[D9]	Schaltbild_Stückliste_BCO CL2 BE 24.pdf	Circuit diagram / parts list “BCO CL2 BE 24” of 23.04.19
[D10]	Schaltbild_Stückliste_BCO CL2 BE 48.pdf	Circuit diagram / parts list “BCO CL2 BE 48” of 23.04.19
[D11]	Schaltbild_Stückliste_BCO ML2 BD 12.pdf	Circuit diagram / parts list “BCO ML2 BD 12” of 07.11.19
[D12]	Schaltbild_Stückliste_BCO ML2 BD 24.pdf	Circuit diagram / parts list “BCO ML2 BD 24” of 07.11.19
[D13]	Schaltbild_Stückliste_BCO ML2 BD 48.pdf	Circuit diagram / parts list “BCO ML2 BD 48” of 07.11.19
[D14]	Schaltbild_Stückliste_BCO ML2 BD EX 24.pdf	Circuit diagram / parts list “BCO ML2 BD EX 24” of 07.11.19
[D15]	Schaltbild_Stückliste_BCO ML2 BD HF 5.pdf	Circuit diagram / parts list “BCO ML2 BD HF 5” of 23.04.19
[D16]	Schaltbild_Stückliste_BCO ML2 BE HF 5.pdf	Circuit diagram / parts list “BCO ML2 BE HF 5” of 23.04.19
[D17]	Schaltbild_Stückliste_BCO ML2 B 180.pdf	Circuit diagram / parts list “BCO ML2 B 180” of 23.04.19
[D18]	Schaltbild_Stückliste_BCO ML2 BE 12.pdf	Circuit diagram / parts list “BCO ML2 BE 12” of 23.04.19
[D19]	Schaltbild_Stückliste_BCO ML2 BE 24.pdf	Circuit diagram / parts list “BCO ML2 BE 24” of 23.04.19
[D20]	Schaltbild_Stückliste_BCO ML2 BE 48.pdf	Circuit diagram / parts list “BCO ML2 BE 48” of 23.04.19
[D21]	Stückliste BCO ML2 MVG 230.pdf	Circuit diagram / parts list “BCO ML2 MVG 230” of 02.02.20
[D22]	SLP 927 214 000 00.pdf	Circuit diagram / parts list “BCO ML2 BPD 24” of September 2021
[D23]	SLP 927 227 000 00.pdf	Circuit diagram / parts list “BCO ML2 BE 180” of September 2021
[D24]	SLP 927 247 000 00.pdf	Circuit diagram / parts list “BCO ML2 BD 180” of September 2021
[D25]	SLP 927 274 000 00.pdf	Circuit diagram / parts list “BCO ML2 BE HF 24” of September 2021
[D26]	SLP 927 275 000 00.pdf	Circuit diagram / parts list “BCO ML2 BD HF 24” of September 2021
[D27]	SLP 927408 000 00.pdf	Circuit diagram / parts list “BCO CL2 BD HC10A 24” of 26.01.2021

[D28]	Overview BCO Series_2024-05-14.pdf	Circuit diagram and parts list for the new types BCO CL2 E 12 / 34 / 48, BCO CL4 BC 24 and BCO ML2 BD HC5A 24 of 14.05.2024
[D29]	Description BCO Series_2024-05-14.pdf	Description for the new types BCO CL2 E 12 / 34 / 48, BCO CL4 BC 24 and BCO ML2 BD HC5A 24 of 14.05.2024

The list above only means that the referenced documents were provided as basis for the FMEDA but it does not mean that *exida* checked the correctness and completeness of these documents.

2.4.2 Documentation generated by *exida*

[R1]	FMEDA_V8_BCO_CL2_B_180.efm V0R1 of 21.10.2019
[R2]	FMEDA_V8_BCO_CL2_B_180_w_ED.efm V0R1 of 21.10.2019
[R3]	FMEDA_V8_BCO_CL2_BD_12-24-48.efm V0R2 of 21.11.2019
[R4]	FMEDA_V8_BCO_CL2_BD_12-24-48_w_ED.efm V0R2 of 21.11.2019
[R5]	FMEDA_V8_BCO_CL2_BD_EX-24.efm V0R2 of 21.11.2019
[R6]	FMEDA_V8_BCO_CL2_BD_EX-24_w_ED.efm V0R2 of 21.11.2019
[R7]	FMEDA_V8_BCO_CL2_BD_HF-5.efm V0R1 of 18.10.2019
[R8]	FMEDA_V8_BCO_CL2_BD_HF-5_w_ED.efm V0R1 of 18.10.2019
[R9]	FMEDA_V8_BCO_CL2_BE_12-24-48.efm V0R1 of 19.09.2019
[R10]	FMEDA_V8_BCO_CL2_BE_12-24-48_w_ED.efm V0R1 of 19.09.2019
[R11]	FMEDA_V8_BCO_CL2_BE_HF-5.efm V0R1 of 19.09.2019
[R12]	FMEDA_V8_BCO_CL2_BE_HF-5_w_ED.efm V0R1 of 19.09.2019
[R13]	FMEDA_V8_BCO_ML2_B_180.efm V0R1 of 21.10.2019
[R14]	FMEDA_V8_BCO_ML2_B_180_w_ED.efm V0R1 of 21.10.2019
[R15]	FMEDA_V8_BCO_ML2_BD_12-24-48.efm V0R2 of 21.11.2019
[R16]	FMEDA_V8_BCO_ML2_BD_12-24-48_w_ED.efm V0R2 of 21.11.2019
[R17]	FMEDA_V8_BCO_ML2_BD_EX-24.efm V0R2 of 21.11.2019
[R18]	FMEDA_V8_BCO_ML2_BD_EX-24_w_ED.efm V0R2 of 21.11.2019

[R19]	FMEDA_V8_BCO_ML2_BD_HF-5.efm V0R1 of 18.10.2019
[R20]	FMEDA_V8_BCO_ML2_BD_HF-5_w_ED.efm V0R1 of 18.10.2019
[R21]	FMEDA_V8_BCO_ML2_BE_12-24-48.efm V0R1 of 19.09.2019
[R22]	FMEDA_V8_BCO_ML2_BE_12-24-48_w_ED.efm V0R1 of 19.09.2019
[R23]	FMEDA_V8_BCO_ML2_BE_HF-5.efm V0R1 of 21.10.2019
[R24]	FMEDA_V8_BCO_ML2_BE_HF-5_w_ED.efm V0R1 of 21.10.2019
[R25]	FMEDA_V8_BCO_ML2_MVG_230.efm V0R1 of 06.04.2021
[R26]	FMEDA_V8_BCO_ML2_MVG_230_w_ED.efm V0R1 of 06.04.2021
[R27]	FMEDA_V8_BCO_ML2_BPD_24.efm
[R28]	FMEDA_V8_BCO_ML2_BPD_24_w_ED.efm
[R29]	FMEDA_V8_BCO_ML2_BE_180.efm
[R30]	FMEDA_V8_BCO_ML2_BE_180_w_ED.efm
[R31]	FMEDA_V8_BCO_ML2_BD_180.efm
[R32]	FMEDA_V8_BCO_ML2_BD_180_w_ED.efm
[R33]	FMEDA_V8_BCO_ML2_BE_HF_24.efm
[R34]	FMEDA_V8_BCO_ML2_BE_HF_24_w_ED.efm
[R35]	FMEDA_V8_BCO_ML2_BD_HF_24.efm
[R36]	FMEDA_V8_BCO_ML2_BD_HF_24_w_ED.efm
[R37]	Printout_FMEDA_V10_BCO_CL2_BD_HC10A_24_V1R1.xlsx
[R38]	Printout_FMEDA_V10_BCO_CL2_BD_HC10A_24_w_ED_V1R1.xlsx
[R39]	Printout_FMEDA_V10_BCO_CL2_E_12_24_48_V1R1.xlsx
[R40]	Printout_FMEDA_V10_BCO_CL2_E_12_24_48_w_ED_V1R1.xlsx
[R41]	Printout_FMEDA_V10_BCO_CL4_BC_24_V1R1.xlsx
[R42]	Printout_FMEDA_V10_BCO_CL4_BC_24_w_ED_V1R1.xlsx
[R43]	Printout_FMEDA_V10_BCO_ML2_BD_HC5A_24_V1R1.xlsx
[R44]	Printout_FMEDA_V10_BCO_ML2_BD_HC5A_24_w_ED_V1R1.xlsx

3 Description of the analyzed devices

BLITZDUCTORconnect are pluggable or compact 2-pole universal lightning current and surge arresters for DIN rail mounting in measuring and control circuits, bus systems, alarm systems and telecommunication systems which are subject to maximum availability requirements.

Integrated LifeCheck monitors the status of the Surge Protective Device (SPD) function and an indicator at the modules shows a defect of the SPD for a quick and easy optical testing without additional test devices. In case of an overload of the SPD the signal circuit will still be available due to the fail-open defect mode. An optional remote signaling unit DEHNrecord monitors the status of an SPD group and signals the status with an integrated remote signaling contact (nc).

The FMEDA of the BCO CL2 / CL4 / ML2 surge arrester series has been carried out on the parts indicated in Figure 1 to Figure 12.

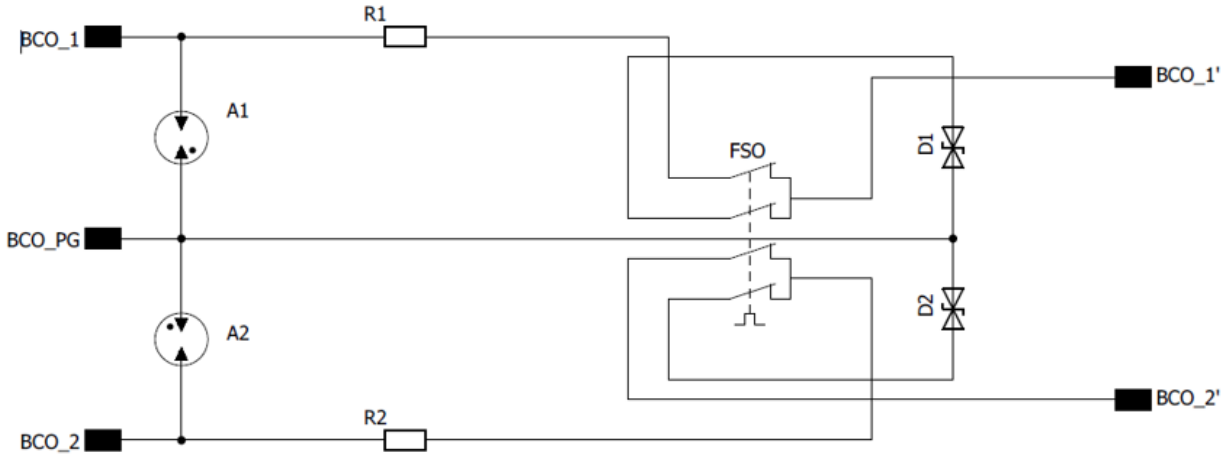


Figure 1: BCO *L2 BE 12, BCO *L2 BE 24, BCO *L2 BE 48, BCO ML2 BE 180

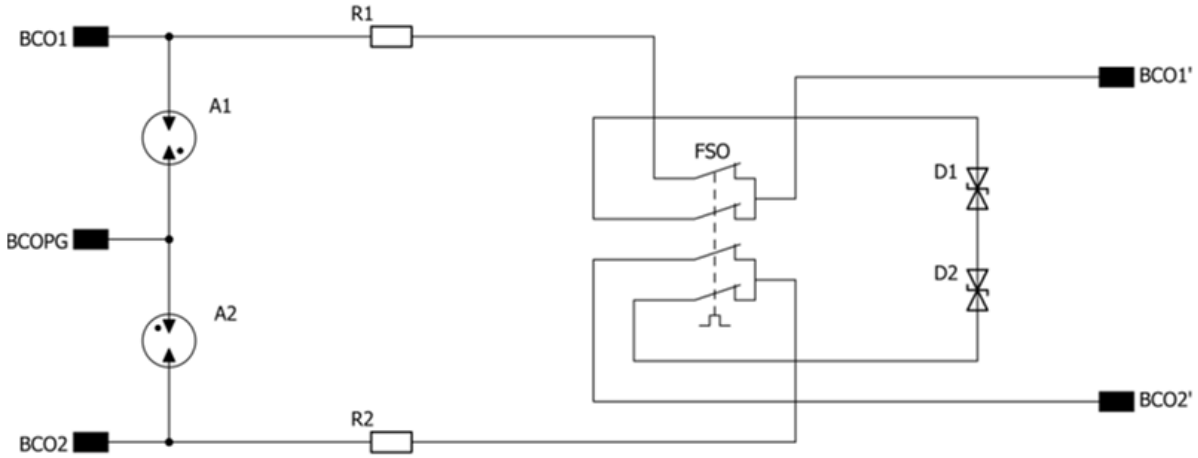


Figure 2: BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48, BCO ML2 BD 180

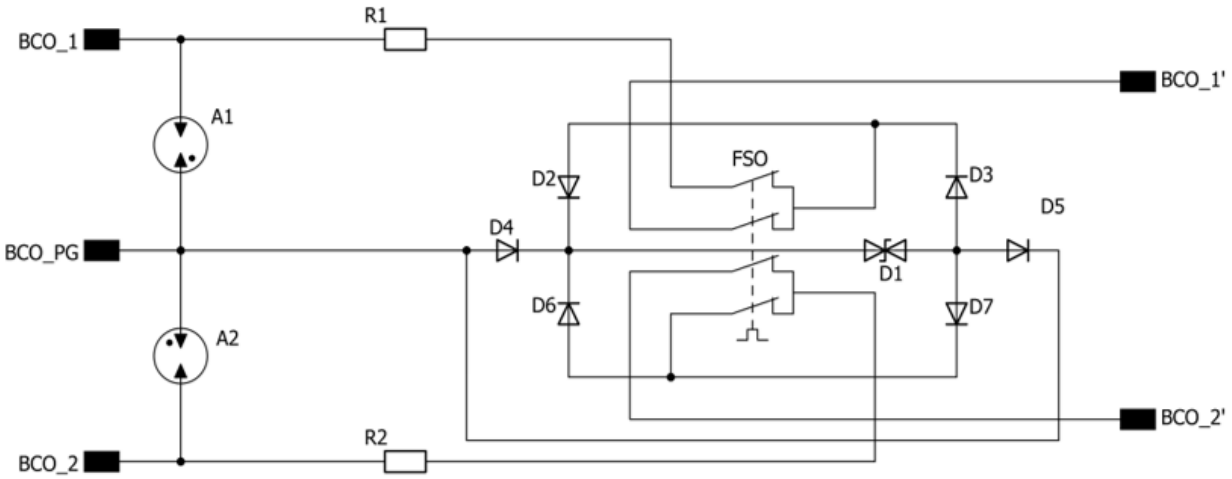


Figure 3: BCO *L2 BE HF 5, BCO ML2 BE HF 24

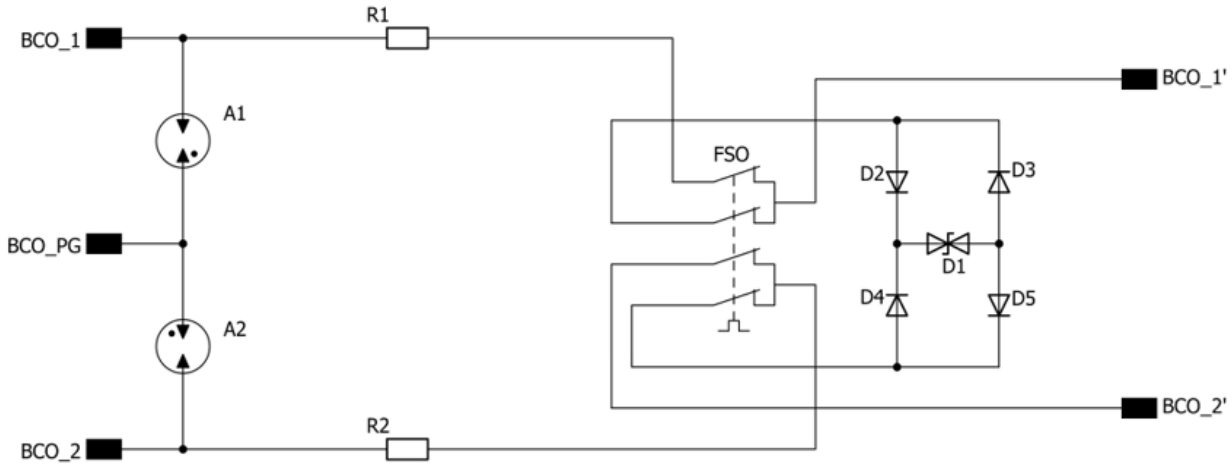


Figure 4: BCO *L2 BD HF 5, BCO ML2 BD HF 24

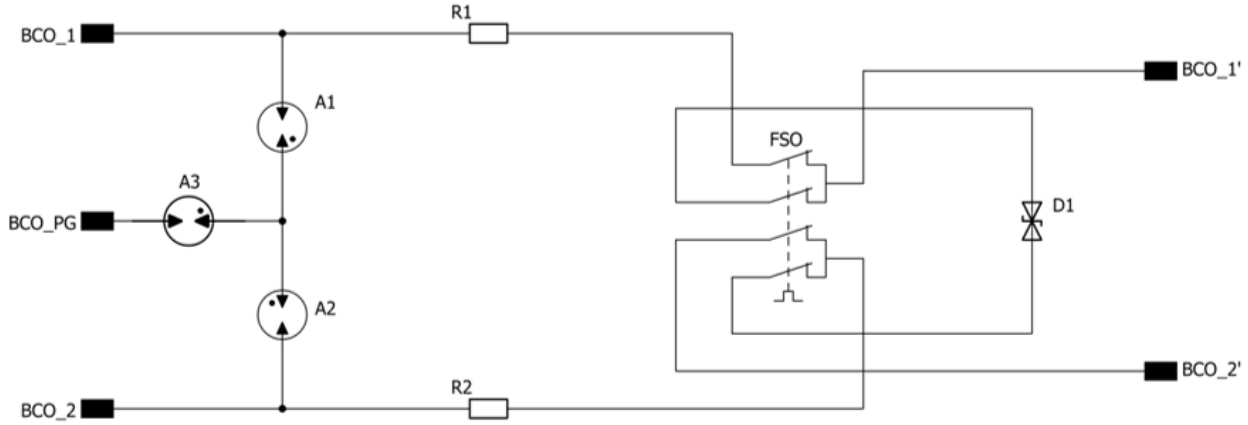


Figure 5: BCO *L2 BD EX 24

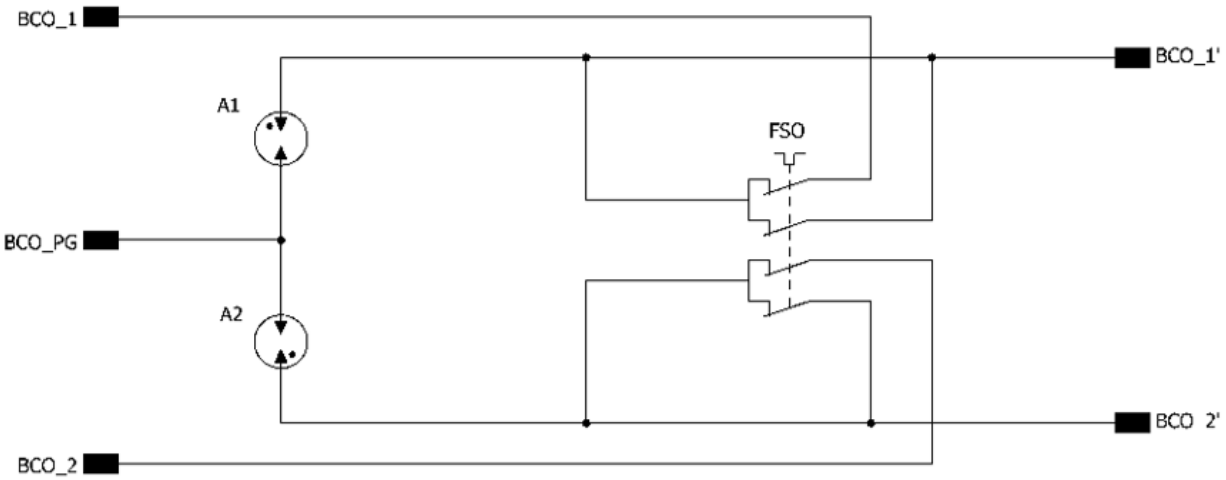


Figure 6: BCO *L2 B 180

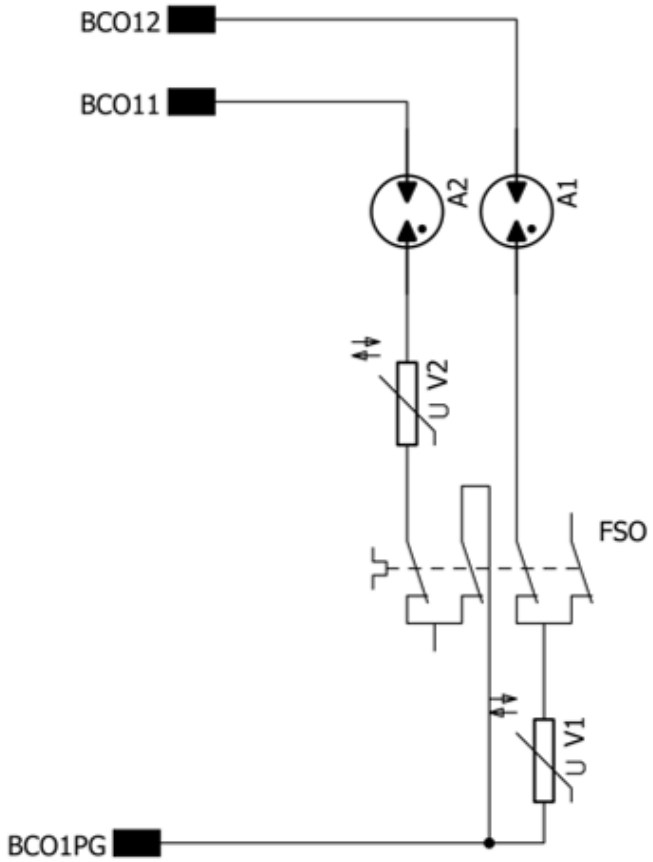


Figure 7: BCO ML2 MVG 230

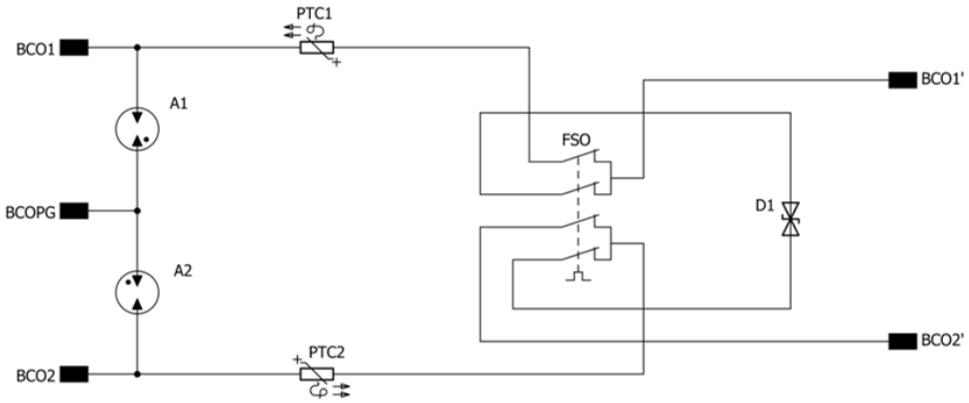


Figure 8: BCO ML2 BPD 24

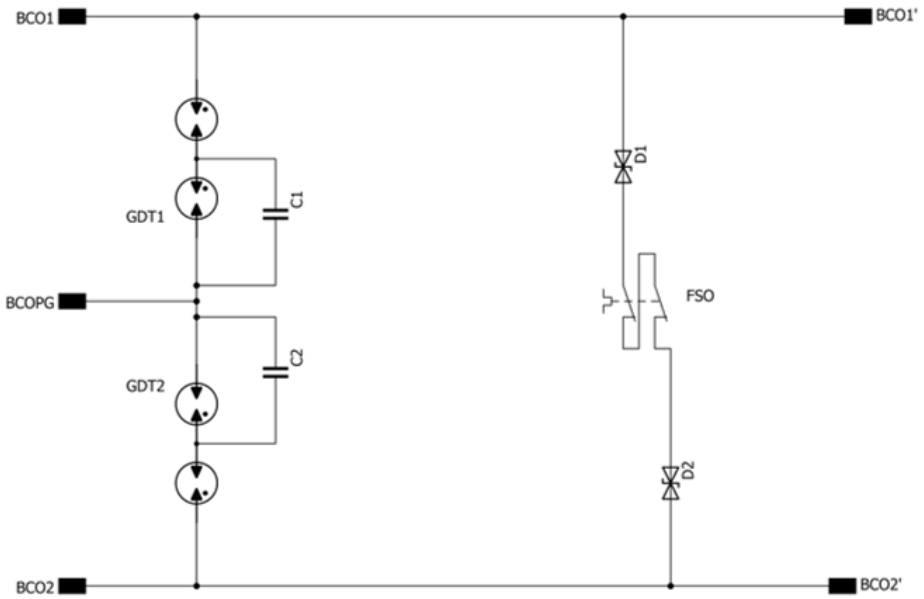


Figure 9: BCO CL2 BD HC10A 24

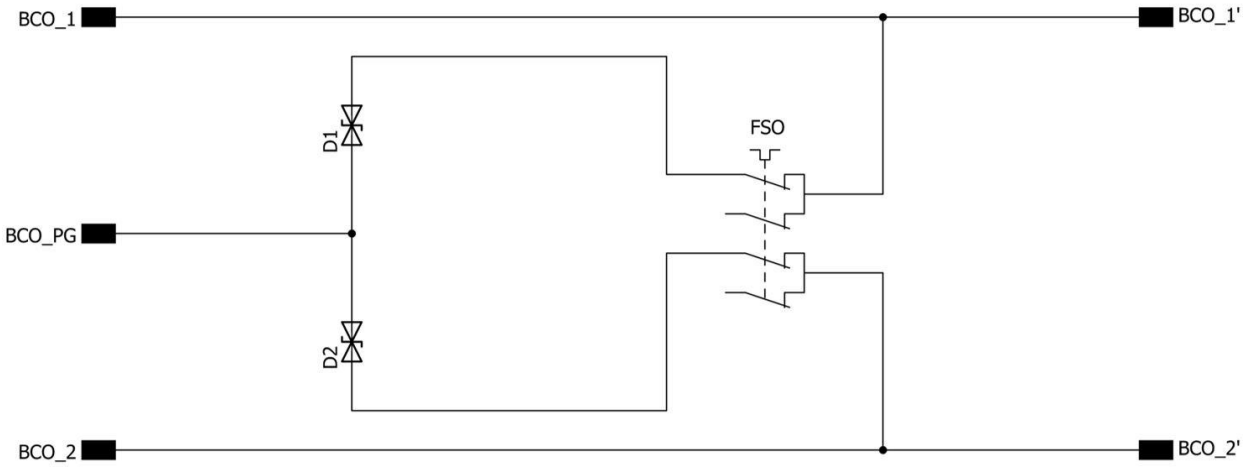


Figure 10: BCO CL2 E 12 / 24 / 48

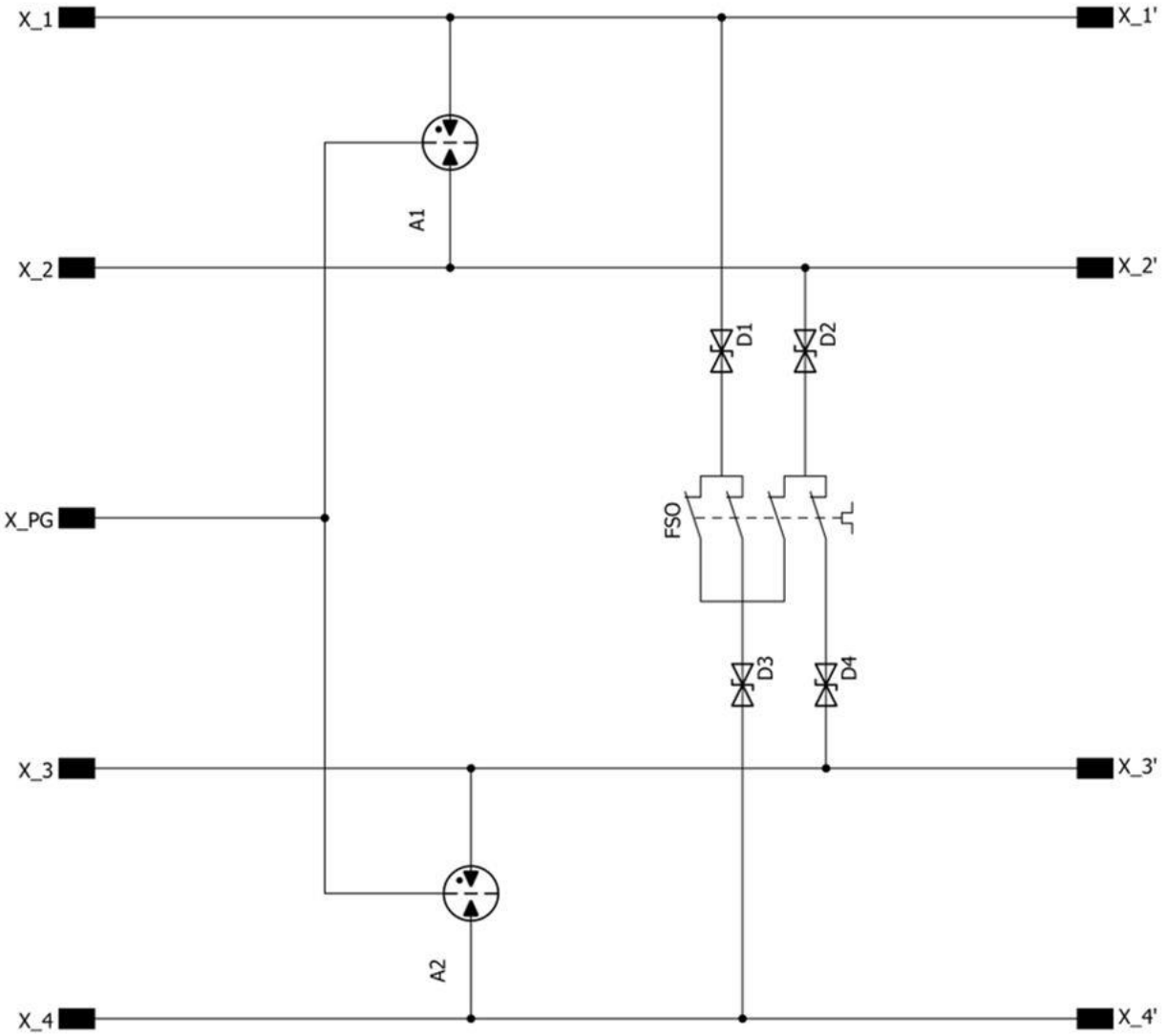


Figure 11: BCO CL4 BC 24

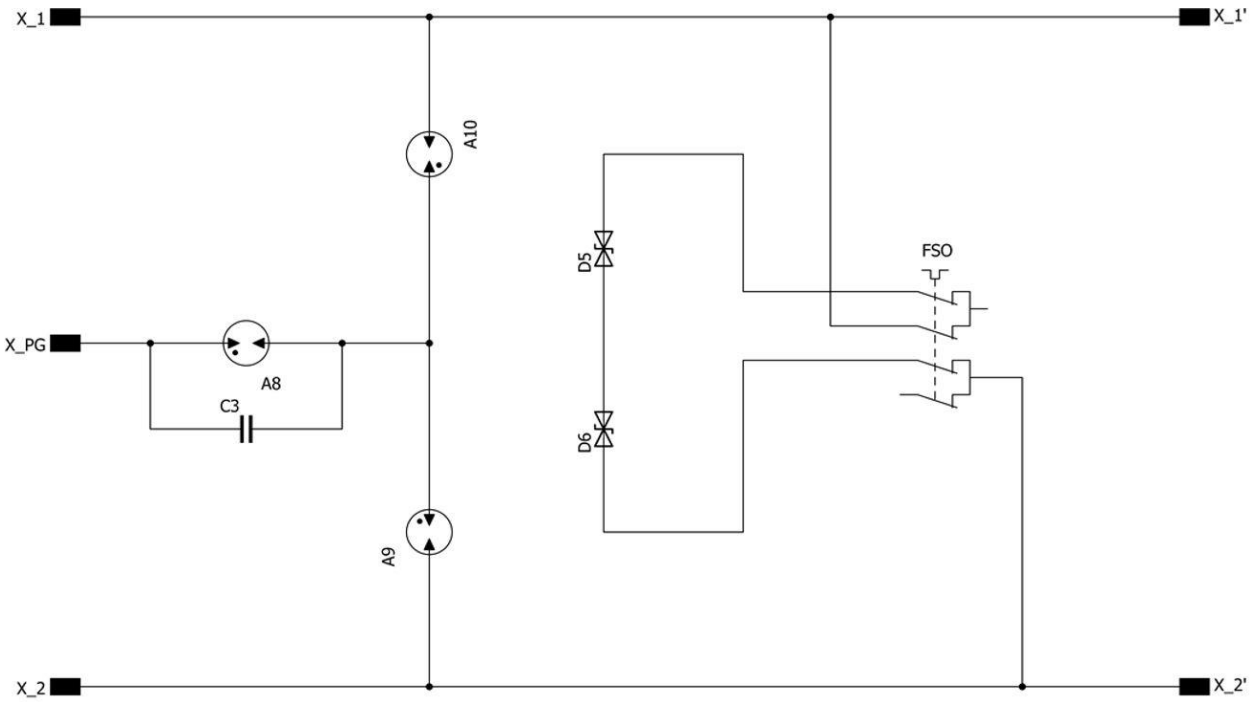


Figure 12: BCO ML2 BD HC5A 24

The following Figure 13 shows how the surge protective devices can be connected to other devices. All considered surge protective devices can be used with analog or binary devices.

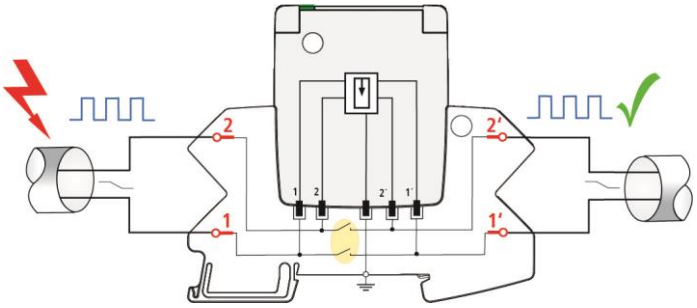


Figure 13: Connection diagram

4 Failure Modes, Effects, and Diagnostic Analysis

The Failure Modes, Effects, and Diagnostic Analysis was done together with DEHN SE + Co KG and is documented in [R1] to [R44]. Failures have been classified according to the following failure categories.

4.1 Description of the failure categories

In order to judge the failure behavior of the BCO CL2 / CL4 / ML2 surge arrester series, the following definitions for the failure of the product were considered.

Fail-Safe State	The fail-safe state is defined as the output being de-energized (when used with binary devices) or reaching the user defined threshold value (when used with analog devices).
Safe	A safe failure (S) is defined as a failure that plays a part in implementing the safety function that: a) results in the spurious operation of the safety function to put the EUC (or part thereof) into a safe state or maintain a safe state; or, b) increases the probability of the spurious operation of the safety function to put the EUC (or part thereof) into a safe state or maintain a safe state.
Dangerous	A dangerous failure (D) is defined as a failure that plays a part in implementing the safety function that: a) prevents a safety function from operating when required (demand mode) or causes a safety function to fail (continuous mode) such that the EUC is put into a hazardous or potentially hazardous state; or, b) decreases the probability that the safety function operates correctly when required.
Dangerous Undetected	Failure that is dangerous and that is not being diagnosed by external diagnostics (DU).
Dangerous Detected	Failure that is dangerous but is detected by external diagnostics (DD).
No effect	Failure mode of a component that plays a part in implementing the safety function but is neither a safe failure nor a dangerous failure.
No part	Component that plays no part in implementing the safety function but is part of the circuit diagram and is listed for completeness.

4.2 Methodology – FMEDA, Failure rates

4.2.1 FMEDA

A Failure Modes and Effects Analysis (FMEA) is a systematic way to identify and evaluate the effects of different component failure modes, to determine what could eliminate or reduce the chance of failure, and to document the system in consideration.

A FMEDA (Failure Modes, Effects, and Diagnostic Analysis) is a FMEA extension. It combines standard FMEA techniques with extension to identify online diagnostics techniques and the failure modes relevant to safety instrumented system design. It is a technique recommended to generate failure rates for each important category (safe detected, safe undetected, dangerous detected, dangerous undetected, fail high, fail low) in the safety models. The format for the FMEDA is an extension of the standard FMEA format from MIL STD 1629A, Failure Modes and Effects Analysis.

4.2.2 Failure rates

The failure rate data used by *exida* in this FMEDA is from the Electrical and Mechanical Component Reliability Handbooks [N2] which was derived using over 200 billion unit operational hours of field failure data from multiple sources and failure data from various databases. The rates were chosen in a way that is appropriate for safety integrity level verification calculations. The rates were chosen to match *exida* Profile 1 (Cabinet mounted / Climate Controlled), see Appendix 3: *exida* Environmental Profiles. The *exida* profile chosen was judged to be the best fit for the product and application information submitted by DEHN SE + Co KG. It is expected that the actual number of field failures due to random events will be less than the number predicted by these failure rates.

For hardware assessment according to IEC 61508 only random equipment failures are of interest. It is assumed that the equipment has been properly selected for the application and is adequately commissioned such that early life failures (infant mortality) may be excluded from the analysis.

Failures caused by external events should be considered as random failures. Examples of such failures are loss of power, physical abuse, or problems due to intermittent instrument air or hydraulic fluid quality.

The assumption is also made that the equipment is maintained per the requirements of IEC 61508 or IEC 61511 and therefore a preventative maintenance program is in place to replace equipment before the end of its “useful life”.

The user of these numbers is responsible for determining their applicability to any particular environment. *exida* Environmental Profiles listing expected stress levels can be found in Appendix 3: *exida* Environmental Profiles. Some industrial plant sites have high levels of stress. Under those conditions the failure rate data is adjusted to a higher value to account for the specific conditions of the plant.

Accurate plant specific data may be used for this purpose. If a user has data collected from a good proof test reporting system such as *exida* SILStat™ that indicates higher failure rates, the higher numbers shall be used.

4.3 Assumptions

The following assumptions have been made during the Failure Modes, Effects, and Diagnostic Analysis of the BCO CL2 / CL4 / ML2 surge arrester series.

- Failure rates are constant, wear out mechanisms are not included.
- Propagation of failures is not relevant.
- The device is installed per manufacturer's instructions.
- The device is used within its specified limits.
- Complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.
- Sufficient tests are performed prior to shipment to verify the absence of vendor and/or manufacturing defects that prevent proper operation of specified functionality to product specifications or cause operation different from the design analyzed.
- For safety applications only the described configurations are considered.
- In case of multiple channel devices only one channel is part of the considered safety function.
- External power supply failure rates are not included.
- The mean time to restoration (MTTR) after a safe failure is 24 hours.
- All modules are operated in the low demand mode of operation.

4.4 Results

For the calculation of the Safe Failure Fraction (SFF) the following has to be noted:

λ_{total} consists of the sum of all component failure rates. This means:

$\lambda_{total} = \lambda_{SD} + \lambda_{SU} + \lambda_{DD} + \lambda_{DU}$

$MTBF = MTTF + MTTR = (1 / (\lambda_{total} + \lambda_{no\ effect} + \lambda_{no\ part})) + 24\ h$

4.4.1 BCO *L2 BE 12, BCO *L2 BE 24, BCO *L2 BE 48, BCO ML2 BE 180

The FMEDA carried out on the BCO *L2 BE 12, BCO *L2 BE 24, BCO *L2 BE 48, BCO ML2 BE 180 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [19]	**Analysis 2** [20]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**7**
Fail Dangerous Undetected (λ_{DU})	**10**	**3**
No effect	37	37
No part	1	1
Total failure rate	**13 FIT**	**13 FIT**
MTBF	**2269 years**	**2269 years**

[19] Analysis 1 represents a worst-case analysis.

[20] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.2 BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48, BCO ML2 BD 180

The FMEDA carried out on the BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48, BCO ML2 BD 180 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [21]	**Analysis 2** [22]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**2**
Fail Dangerous Undetected (λ_{DU})	**10**	**8**
No effect	37	37
No part	1	1
Total failure rate	**13 FIT**	**13 FIT**
MTBF	**2269 years**	**2269 years**

[21] Analysis 1 represents a worst-case analysis.

[22] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.3 BCO *L2 BE HF 5, BCO ML2 BE HF 24

The FMEDA carried out on the BCO *L2 BE HF 5 and BCO ML2 BE HF 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [23]	**Analysis 2** [24]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**17**
Fail Dangerous Undetected (λ_{DU})	**20**	**3**
No effect	48	48
No part	1	2
Total failure rate	**23 FIT**	**23 FIT**
MTBF	**1601 years**	**1601 years**

[23] Analysis 1 represents a worst-case analysis.

[24] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.4 BCO *L2 BD HF 5, BCO ML2 BD HF 24

The FMEDA carried out on the BCO *L2 BD HF 5 and BCO ML2 BD HF 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [25]	**Analysis 2** [26]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**13**
Fail Dangerous Undetected (λ_{DU})	**16**	**3**
No effect	44	44
No part	1	1
Total failure rate	**19 FIT**	**19 FIT**
MTBF	**1803 years**	**1803 years**

[25] Analysis 1 represents a worst-case analysis.

[26] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.5 BCO *L2 BD EX 24

The FMEDA carried out on the BCO *L2 BD EX 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	exida Profile 1	
	Analysis 1 [27]	**Analysis 2** [28]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**6**
Fail Dangerous Undetected (λ_{DU})	**10**	**4**
No effect	54	54
No part	1	1
Total failure rate	**13 FIT**	**13 FIT**
MTBF	**1696 years**	**1696 years**

[27] Analysis 1 represents a worst-case analysis.

[28] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.6 BCO *L2 B 180

The FMEDA carried out on the BCO *L2 B 180 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [29]	**Analysis 2** [30]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**2**
Fail Dangerous Undetected (λ_{DU})	**4**	**2**
No effect	36	36
No part	1	1
Total failure rate	**6 FIT**	**6 FIT**
MTBF	**2686 years**	**2686 years**

[29] Analysis 1 represents a worst-case analysis.

[30] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.7 BCO ML2 MVG 230

The FMEDA carried out on the BCO ML2 MVG 230 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [31]	**Analysis 2** [32]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**6**	**2**
No effect	42	42
No part	1	1
Total failure rate	**8 FIT**	**8 FIT**
MTBF	**2261 years**	**2261 years**

[31] Analysis 1 represents a worst-case analysis.

[32] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.8 BCO ML2 BPD 24

The FMEDA carried out on the BCO ML2 BPD 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [33]	**Analysis 2** [34]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**8**	**8**
Fail Dangerous Detected (λ_{DD})	**0**	**2**
Fail Dangerous Undetected (λ_{DU})	**11**	**9**
No effect	36	36
No part	1	1
Total failure rate	**19 FIT**	**19 FIT**
MTBF	**2057 years**	**2057 years**

[33] Analysis 1 represents a worst-case analysis.

[34] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.9 BCO CL2 BD HC10A 24

The FMEDA carried out on the BCO CL2 BD HC10A 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	exida Profile 1	
	Analysis 1 [35]	**Analysis 2** [36]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**8**
Fail Dangerous Undetected (λ_{DU})	**12**	**4**
No effect	73	73
No part	4	4
Total failure rate	**14 FIT**	**14 FIT**
MTBF	**1273 years**	**1273 years**

[35] Analysis 1 represents a worst-case analysis.

[36] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.10 BCO CL2 E 12 / 24 / 48

The FMEDA carried out on the BCO CL2 E 12 / 24 / 48 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	***exida* Profile 1**	
	Analysis 1 [37]	**Analysis 2** [38]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**5**
Fail Dangerous Undetected (λ_{DU})	**6**	**1**
No effect	1	1
No part	1	1
Total failure rate	**8 FIT**	**8 FIT**
MTBF	**13430 years**	**13430 years**

[37] Analysis 1 represents a worst-case analysis.

[38] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.11 BCO CL4 BC 24

The FMEDA carried out on the BCO CL4 BC 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	exida Profile 1	
	Analysis 1 [39]	**Analysis 2** [40]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**10**
Fail Dangerous Undetected (λ_{DU})	**13**	**3**
No effect	37	37
No part	4	4
Total failure rate	**16 FIT**	**16 FIT**
MTBF	**2020 years**	**2020 years**

[39] Analysis 1 represents a worst-case analysis.

[40] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

4.4.12 BCO ML2 BD HC5A 24

The FMEDA carried out on the BCO ML2 BD HC5A 24 surge arresters leads under the assumptions described in sections 4.3 and 4.4 and the definitions given in section 4.1 to the following failure rates:

	exida Profile 1	
	Analysis 1 [41]	**Analysis 2** [42]
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**5**
Fail Dangerous Undetected (λ_{DU})	**7**	**2**
No effect	36	36
No part	24	24
Total failure rate	**9 FIT**	**9 FIT**
MTBF	**1657 years**	**1657 years**

[41] Analysis 1 represents a worst-case analysis.

[42] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

5 Using the FMEDA results

It is the responsibility of the Safety Instrumented Function designer to do calculations for the entire SIF. *exida* recommends the accurate Markov based exSILentia tool for this purpose.

The following section describes how to apply the results of the FMEDA.

5.1 Example PFD_{AVG} / PFH calculation

The following results must be considered in combination with PFD_{AVG} / PFH values of other devices of a Safety Instrumented Function (SIF) in order to determine suitability for a specific Safety Integrity Level (SIL).

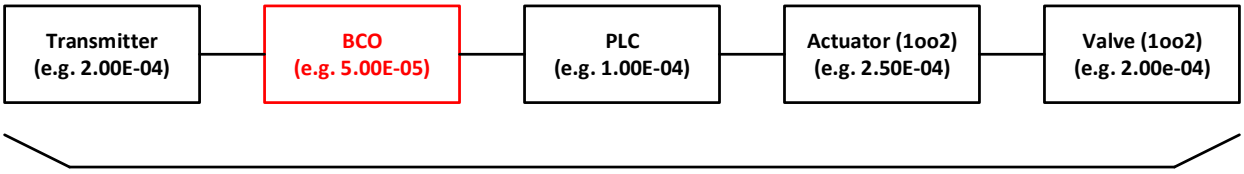
An average Probability of Failure on Demand (PFD_{AVG}) calculation is performed for a single (1oo1) surge protective device with *exida's* exSILentia tool. The failure rate data used in this calculation are displayed in sections 4.4.1 to 4.4.6 for analysis 2. A mission time of 10 years has been assumed, a Mean Time To Restoration of 24 hours and a maintenance capability of 100%.

Table 14 and Table 15 list the results of all devices considering a proof test coverage of 99% (see Appendix 1.1) for the PFD_{AVG} calculation.

For SIL2 the overall PFD_{AVG} shall be better than 1.00E-02 and the PFH shall be better than 1.00E-06 1/h.

For SIL3 the overall PFD_{AVG} shall be better than 1.00E-03 and the PFH shall be better than 1.00E-07 1/h.

As the surge protective devices are contributing to the entire safety function they should only consume a certain percentage of the allowed range. Assuming 5% of this range as a reasonable budget they should be better than or equal to 5.00E-04 or 5.00E-08 1/h, respectively for SIL2 and better than or equal to 5.00E-05 or 5.00E-09 1/h, respectively for SIL3. Figure 14 illustrates this on an example.



SIL2: PFD_{AVG} < 1.00E-02

SIL3: PFD_{AVG} < 1.00E-03

Example: PFD_{AVG} = 8.00E-04 < 1.00E-03

Figure 14: SIF example

Table 14 and Table 15 show that the calculated PFD_{AVG} / PFH values are within the allowed range for SIL 2 / SIL 3 according to table 2 of IEC 61508-1 and their contribution to the SIL budget. Most of the devices fulfill the assumption to not claim more than 5% of the allowed range.

Table 14: PFD_{AVG}

Type	T[Proof] = 1 year	Percentage of SIL2	Percentage of SIL3
BCO *L2 BE 12, BCO *L2 BE 24, BCO *L2 BE 48, BCO ML2 BE 180	PFD_{AVG} = 1.45E-05	≈ 0.1%	≈ 1%
BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48, BCO ML2 BD 180	PFD_{AVG} = 3.82E-05	≈ 0.4%	≈ 4%
BCO *L2 BE HF 5, BCO ML2 BE HF 24	PFD_{AVG} = 1.47E-05	≈ 0.1%	≈ 1%
BCO *L2 BD HF 5, BCO ML2 BD HF 24	PFD_{AVG} = 1.46E-05	≈ 0.1%	≈ 1%
BCO *L2 BD EX 24	PFD_{AVG} = 1.92E-05	≈ 0.2%	≈ 2%
BCO *L2 B 180	PFD_{AVG} = 9.58E-06	≈ 0.1%	≈ 1%
BCO ML2 MVG 230	PFD_{AVG} = 9.60E-06	≈ 0.1%	≈ 1%
BCO ML2 BPD 24	PFD_{AVG} = 4.17E-05	≈ 0.4%	≈ 4%
BCO CL2 BD HC10A 24	PFD_{AVG} = 2.40E-05	≈ 0.2%	≈ 2%
BCO CL2 E 12 / 24 / 48	PFD_{AVG} = 2.14E-06	≈ 0%	≈ 0.2%
BCO CL4 BC 24	PFD_{AVG} = 1.46E-05	≈ 0.1%	≈ 1%
BCO ML2 BD HC5A 24	PFD_{AVG} = 1.25E-05	≈ 0.1%	≈ 1%

Table 15: PFH values

Type	PFH	Percentage of SIL2	Percentage of SIL3
BCO *L2 BE 12, BCO *L2 BE 24, BCO *L2 BE 48, BCO ML2 BE 180	PFH = 3.10E-09 1/h	≈ 0.3%	≈ 3%
BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48, BCO ML2 BD 180	PFH = 8.14E-09 1/h	≈ 0.8%	≈ 8%
BCO *L2 BE HF 5, BCO ML2 BE HF 24	PFH = 3.04E-09 1/h	≈ 0.3%	≈ 3%
BCO *L2 BD HF 5, BCO ML2 BD HF 24	PFH = 3.00E-09 1/h	≈ 0.3%	≈ 3%
BCO *L2 BD EX 24	PFH = 3.93E-09 1/h	≈ 0.4%	≈ 4%
BCO *L2 B 180	PFH = 2.02E-09 1/h	≈ 0.2%	≈ 2%
BCO ML2 MVG 230	PFH = 2.04E-09 1/h	≈ 0.2%	≈ 2%
BCO ML2 BPD 24	PFH = 8.72E-09 1/h	≈ 0.9%	≈ 9%
BCO CL2 BD HC10A 24	PFH = 4.23E-09 1/h	≈ 0.4%	≈ 4%
BCO CL2 E 12 / 24 / 48	PFH = 3.55E-10 1/h	≈ 0%	≈ 0.3%
BCO CL4 BC 24	PFH = 2.55E-09 1/h	≈ 0.3%	≈ 3%
BCO ML2 BD HC5A 24	PFH = 2.20E-09 1/h	≈ 0.2%	≈ 2%

The resulting PFD_{AVG} graph for a single (1oo1) surge arrester BCO *L2 BD 12, BCO *L2 BD 24, BCO *L2 BD 48 (representing the worst-case of all considered devices) generated from the exSILentia tool for a proof test of 1 year is displayed in

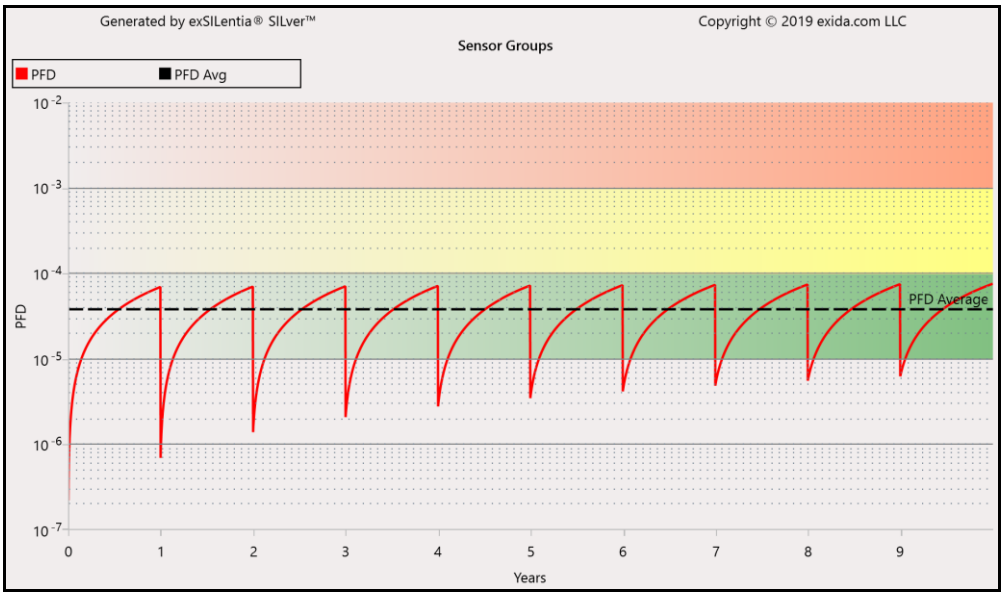


Figure 15: $PFD_{AVG}(t)$

6 Terms and Definitions

FIT	Failure In Time ($1x10^{-9}$ failures per hour)
FMEDA	Failure Modes, Effects, and Diagnostic Analysis
HFT	Hardware Fault Tolerance
High demand mode	Mode, where the safety function is only performed on demand, in order to transfer the EUC into a specified safe state, and where the frequency of demands is greater than one per year.
Low demand mode	Mode, where the safety function is only performed on demand, in order to transfer the EUC into a specified safe state, and where the frequency of demands is no greater than one per year.
PFD_{AVG}	Average Probability of Failure on Demand
PFH	Probability of dangerous Failure per Hour
SFF	Safe Failure Fraction summarizes the fraction of failures which lead to a safe state and the fraction of failures which will be detected by diagnostic measures and lead to a defined safety action.
SIF	Safety Instrumented Function
SIL	Safety Integrity Level
T[Proof]	Proof Test Interval

7 Status of the document

7.1 Liability

exida prepares reports based on methods advocated in International standards. Failure rates are obtained from a collection of industrial databases. *exida* accepts no liability whatsoever for the use of these numbers or for the correctness of the standards on which the general calculation methods are based.

Due to future potential changes in the standards, best available information and best practices, the current FMEDA results presented in this report may not be fully consistent with results that would be presented for the identical product at some future time. As a leader in the functional safety market place, *exida* is actively involved in evolving best practices prior to official release of updated standards so that our reports effectively anticipate any known changes. In addition, most changes are anticipated to be incremental in nature and results reported within the previous three year period should be sufficient for current usage without significant question.

Most products also tend to undergo incremental changes over time. If an *exida* FMEDA has not been updated within the last three years and the exact results are critical to the SIL verification you may wish to contact the product vendor to verify the current validity of the results.

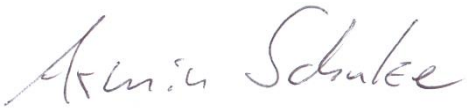
7.2 Releases

Version History:	V4R2	Corrected connector FIT value to 0.5 FIT for BCO CL2 BD HC10A 24, BCO CL2 E 12 / 24 / 48, BCO CL4 BC 24 and BCO ML2 BD HC5A 24; July 11, 2024
	V4R1	Corrected after review by Stephan Aschenbrenner (*exida*); June 05, 2024
	V4R0	BCO CL2 E series, BCO CL4 BC 24 and BCO ML2 BD HC5A 24 Added; June 03, 2024
	V3R0	BCO CL2 BD HC10A 24 added; December 13, 2022
	V2R2	Description of figures extended, figure added; December 13, 2022
	V2R1	Devices BCO ML2 BPD 24, BCO ML2 BE 180, BCO ML2 BD 180, BCO ML2 BE HF 24, BCO ML2 BD HF 24 added; November 11, 2021
	V2R0	Device BCO ML2 MVG 230 added: May 2, 2021
	V1R0	Review comments incorporated; March 16, 2020
	V0R1	Initial version; February 26, 2020
Author:	Armin Schulze, Philipp Hanzik, Jan Hettenbach, Stephan Aschenbrenner	
Review:	V4R2	Stephan Aschenbrenner (*exida*); July 12, 2024
	V4R1	Christian Frey (DEHN SE); July 08, 2024
	V4R0	Stephan Aschenbrenner (*exida*); June 06, 2024
	V0R1	Jan Hettenbach (*exida*); March 13, 2020
		Christian Frey (DEHN SE + Co KG); March 12, 2020
Release status:	Released to DEHN SE	

Release Signatures



Dipl.-Ing. (Univ.) Stephan Aschenbrenner, Partner, CEO



Dipl.-Ing. (Univ.) Armin Schulze, Safety Engineer

Appendix 1: Possibilities to reveal dangerous undetected faults during the proof test

According to section 7.4.5.2 f) of IEC 61508-2 proof tests shall be undertaken to reveal dangerous faults which are undetected by diagnostic tests.

This means that it is necessary to specify how dangerous undetected faults which have been noted during the FMEDA can be detected during proof testing.

Appendix 1 shall be considered when writing the safety manual as it contains important safety related information.

Appendix 1.1: Proof test to detect dangerous undetected faults

A suggested proof test consists of the following steps, as described in Table 16.

Table 16 Steps for a possible proof Test

Step	Action
1	Bypass the connected safety device(s) or take other appropriate action to avoid a false trip
2	Force the BCO CL2 / CL4 / ML2 surge arrester series to reach predefined output signals over the entire range and verify that the output behaves as expected.
3	Restore the loop to full operation
4	Remove the bypass from the connected safety device(s) or otherwise restore normal operation

This test will detect approximately 99% of possible “DU” failures of the BCO CL2 / CL4 / ML2 surge arrester series.

Appendix 2: Impact of lifetime of critical components on the failure rate

According to section 7.4.9.5 of IEC 61508-2, a useful lifetime, based on experience, should be assumed.

Although a constant failure rate is assumed by the probabilistic estimation method (see section 4.3) this only applies provided that the useful lifetime[43] of components is not exceeded. Beyond their useful lifetime the result of the probabilistic calculation method is therefore meaningless, as the probability of failure significantly increases with time. The useful lifetime is highly dependent on the component itself and its operating conditions – temperature in particular (for example, electrolytic capacitors can be very sensitive).

This assumption of a constant failure rate is based on the bathtub curve, which shows the typical behavior for electronic components. Therefore, it is obvious that the PFD_{AVG} calculation is only valid for components which have this constant domain and that the validity of the calculation is limited to the useful lifetime of each component.

It is assumed that early failures are detected to a huge percentage during the installation period and therefore the assumption of a constant failure rate during the useful lifetime is valid.

The BCO CL2 / ML2 surge arrester series do not contain components with reduced useful lifetime which are contributing to the dangerous undetected failure rate and therefore to the PFD_{AVG} calculation. Therefore, there is no limiting factor to the useful lifetime.

When plant experience indicates a shorter useful lifetime than indicated in this appendix, the number based on plant experience should be used.

[43] Useful lifetime is a reliability engineering term that describes the operational time interval where the failure rate of a device is relatively constant. It is not a term which covers product obsolescence, warranty, or other commercial issues.

Appendix 3: *exida* Environmental Profiles

***exida* Profile**	**1**	**2**	**3**	**4**	**5**	**6**
Description (Electrical)	Cabinet mounted/ Climate Controlled	Low Power Field Mounted no self-heating	General Field Mounted self-heating	Subsea	Offshore	N/A
Description (Mechanical)	Cabinet mounted/ Climate Controlled	General Field Mounted	General Field Mounted	Subsea	Offshore	Process Wetted
IEC 60654-1 Profile	B2	C3 also applicable for D1	C3 also applicable for D1	N/A	C3 also applicable for D1	N/A
Average Ambient Temperature	30°C	25°C	25°C	5°C	25°C	25°C
Average Internal Temperature	60°C	30°C	45°C	5°C	45°C	Process Fluid Temp.
Daily Temperature Excursion (pk-pk)	5°C	25°C	25°C	0°C	25°C	N/A
Seasonal Temperature Excursion (winter average vs. summer average)	5°C	40°C	40°C	2°C	40°C	N/A
Exposed to Elements/Weather Conditions	No	Yes	Yes	Yes	Yes	Yes
Humidity[44]	0-95% Non-Condensing	0-100% Condensing	0-100% Condensing	0-100% Condensing	0-100% Condensing	N/A
Shock[45]	10 g	15 g	15 g	15 g	15 g	N/A
Vibration[46]	2 g	3 g	3 g	3 g	3 g	N/A
Chemical Corrosion[47]	G2	G3	G3	G3	G3	Compatible Material
Surge[48]						
Line-Line	0.5 kV	0.5 kV	0.5 kV	0.5 kV	0.5 kV	N/A
Line-Ground	1 kV	1 kV	1 kV	1 kV	1 kV	
EMI Susceptibility[49]						
80MHz to 1.4 GHz	10V /m	10V /m	10V /m	10V /m	10V /m	N/A
1.4 GHz to 2.0 GHz	3V/m	3V/m	3V/m	3V/m	3V/m	
2.0Ghz to 2.7 GHz	1V/m	1V/m	1V/m	1V/m	1V/m	
ESD (Air)[50]	6kV	6kV	6kV	6kV	6kV	N/A

[44] Humidity rating per IEC 60068-2-3
[45] Shock rating per IEC 60068-2-27
[46] Vibration rating per IEC 60068-2-6
[47] Chemical Corrosion rating per ISA 71.04
[48] Surge rating per IEC 61000-4-5
[49] EMI Susceptibility rating per IEC 6100-4-3
[50] ESD (Air) rating per IEC 61000-4-2