

NRG Modbus RTU User Manual

Operating instructions

Manuale d’istruzioni

Betriebsanleitung

Manuel d’instructions

Manual de instrucciones

Brugervejledning

操作说明

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1. Introduction

1.1. Foreword

The NRG described hereafter is a sub-system made up of a number of solid state relays intended for the switching of heaters in a machine. The solid state relays in this system are able to communicate with the main controller through an NRG controller that facilitates communication between the solid state relays and the main controller. The NRG controller is available with various communication interfaces including PROFINET, EtherNet/IP™, EtherCAT, Modbus TCP and Modbus RTU. Through this communication, it is possible for the main controller to control each solid state relay, read measurements related to each specific solid state relay and to identify specific failure modes related to the solid state relay or its associated heater load.

1.2. Scope

This manual is intended to provide information about the functionalities that are provided by the NRG system, explains set-up and configuration procedures, provides recommendations for use and gives a troubleshooting guide.

Should there be any problems that cannot be solved with the information provided in this guide, contact your Carlo Gavazzi sales representative for further assistance.

1.3. Disclaimer

Carlo Gavazzi accepts no liability for any consequence resulting from inappropriate, negligent, incorrect installation or adjustment of parameters of the equipment. Nor can Carlo Gavazzi assume liability for recommendations that appear or are implied in the following description. The information in this document is not considered binding on any product warranty.

The contents of this guide are believed to be correct at the time of publishing. In the interests of commitment to a policy of continuous development and improvement, Carlo Gavazzi reserves the right to change the specification of the product or its performance, or the contents of this guide without prior notice.

1.4. Warning notice system

The symbols indicated below are used throughout this guide to indicate a particularly important subject or information on safety instructions, configuration and installation of the products covered by this guide.
It is strongly recommended that this guide is read thoroughly before using the products and that safety related recommendations are followed.



Danger
Indicates that death, severe personal injury or property damage will result if proper precautions are not taken.



Warning
Indicates actions that if not observed may lead to damage of the products.



Information
Indicates general information related to the proper use of the products.

1.5. Qualified personnel



The product / system described in this documentation may be operated only by personnel qualified for the specific task that are also capable of identifying risks and avoid potential hazards when working with these products.

The NRG system features dangerous voltages and consequently failure to observe the instructions contained in this user manual may cause serious harm to people and damage to property.

1.6. Abbreviations and acronyms

Acronym	Description
RG..N **RG..CM..N** **End-device**	NRG solid state relays
RGx1A..D..N **RGx1A..CM..N**	NRG zero cross switching solid state relay
RGx1P..CM..N	NRG proportional switching solid state relay
RGC2/3P..N	NRG 2/3 pole proportional switching solid state relay
RGC2P..N	NRG 2-pole proportional switching solid state relay
RGC3P..N	NRG 3-pole proportional switching solid state relay
NRGC..	NRG Controller
PLC	Programmable Logic Controller
SSR	Solid State Relay
AUX	Auxiliary
COM	Common
EMR	Electro Mechanical Relay
NC	Normally Closed
NO	Normally Open

In the following document abbreviations are used in reference to registers. In these cases, the last letter of these abbreviations gives an indication to the type of data being referred to. For example:

CTRS**R**	the last letter 'R' refers to a 16-bit Register. CTRSR = Controller (NRGC) Status Register
TPRD**C**	the last letter 'C' refers to a 16-bit Counter. TPRDC = Total Present End-Device Counter
CMMD**B**	the last letter 'B' refers to a set of bits within a Register. CMMDB = Command Bits
CRST**F**	the last letter 'F' refers to a single bit Flag indicating a status. CRSTF = Controller Reset Flag

1.7. Other documentation

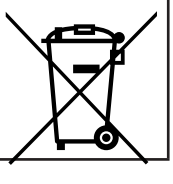
Datasheets, installation guide, certificates and other relevant documentation can be found online at www.gavazziautomation.com

1.8. Disposal

Information for user on the correct handling of waste of electrical and electronic equipment (WEEE)

With reference to European Union directive 2002/96/EC issued on 27 January 2003 and the related national legislation, please note that:

- WEEE cannot be disposed of as municipal waste and such waste must be collected and disposed of separately.
- The public or private waste collection systems defined by local legislation must be used. In addition, the equipment can be returned to the distributor at the end of its working life when buying new equipment.
- The equipment may contain hazardous substances: the improper use or incorrect disposal of such equipment may have negative effects on human health and on the environment.
- The symbol (crossed-out wheelie bin) shown on the product or on the packaging and on the instruction sheet indicates that the equipment has been introduced onto the market after 13th August 2005 and that it must be disposed of separately.
- In the event of illegal disposal of electrical and electronic waste, the penalties are specified by local waste disposal legislation



2. Description

2.1. System overview

The NRG is a sub-system that consists of one or more BUS chains that interact with the main controller or PLC in the machine through a Modbus TCP communication interface. The communication link in the NRG systems can be used to control the solid state relay, monitor various parameters, and diagnose faults in real time.

An NRG BUS chain is made up of a minimum 1x NRG controller and a minimum of 1 x NRG solid state relay (also referred to as end-device). The NRG bus chain can have a maximum of 32 switched poles (1-pole device = 1 switched pole, 2-pole device = 2 switched poles, 3-pole device = 3 switched poles. The 1-pole, 2-pole and 3-pole end-devices can be mixed on one bus chain as long as the 32 switched poles limit is not exceeded. The communication link between the NRG controller and the end-devices is the Internal BUS.

When more solid state relays are needed in a system, multiple BUS chains can be utilised. Each BUS chain connects to another BUS chain in a line topology via the NRG controllers of the respective BUS chains or in a star topology via an Ethernet switch.

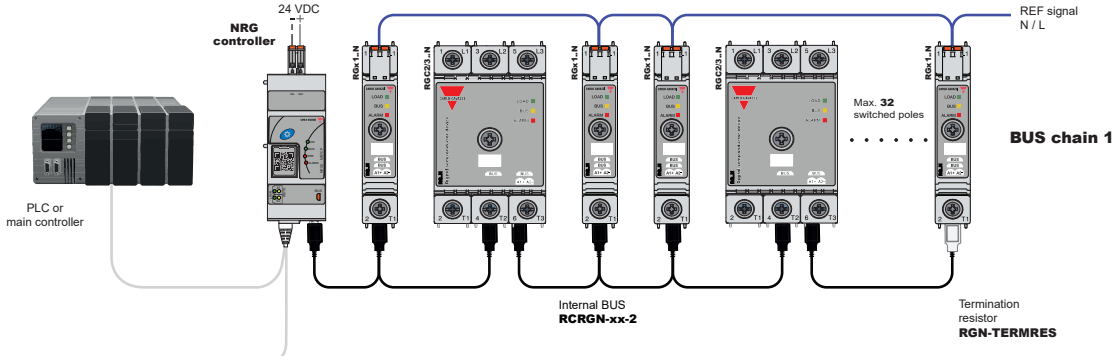


Fig. 1 - NRG bus chain

2.2. System components

The following system components are required for an NRG bus chain:

Description	Part Number	Notes
NRG Controller	NRGC..	**NRGC** NRG Controller with Modbus RTU. **NRGC-PN** NRG controller with PROFINET. **NRGC-EIP** NRG controller with Ethernet/IP™. **NRGC-ECAT** NRG controller with EtherCAT. **NRGC-MBTCP** NRG controller with Modbus TCP. 1x RGN-TERMRES is included in the NRGC.. packaging. The RGN-TERMRES is to be plugged into the last RG..N on the bus chain.

NRG Solid State Relays	RG..CM..N	**RGx1A..D..N** NRG 1-pole zero cross switching solid state relay (no control via communication) **RGx1A..CM..N** NRG 1-pole zero cross switching solid state relay **RGx1P..CM..N** NRG 1-pole proportional switching solid state relay **RGC2P..CM..N** NRG 2-pole proportional switching solid state relay **RGC3P..CM..N** NRG 3-pole proportional switching solid state relay
NRG Internal Bus Cables	RCRGN-xx	Proprietary cables terminated at both ends with micro USB connector

NRG Controller



The NRG controller handles the communication with the higher-level controller and with the NRG solid state relays. It has to be supplied with a 24VDC supply and provides the power supply to the connected NRG solid state relays via the internal bus cables. A termination resistor (RGN-TERMRES) provided with every NRG controller has to be fitted on the last solid state relay of the NRG bus chain. The NRG controller is also capable of performing internal operations to setup and maintain the internal bus.

The NRGC is also equipped with an auxiliary electromagnetic relay (EMR) output that can be wired in a normally open or a normally closed configuration. As a default setting, this auxiliary relay is activated in the presence of an alarm condition, i.e., any alarm condition identified by the NRGC. Through the relay configuration register of the NRGC, it is possible to mask certain alarm conditions and hence have the auxiliary EMR operate only (i.e. change state) under specific alarm conditions (refer to Section 5.2.1 for further details). Through this register it is also possible to change the function of this auxiliary output from an alarm output to a general purpose relay working independently of the NRG system.

Various NRG Controller variants are available which facilitate communication via different communication protocols. These are identified via the part numbers. The NRG controller with communication through Modbus RTU over RS485 is the **NRGC**.

NRG solid state relays



The RGx1..N solid state relays are the switching components in the NRG system. They are available with and without heatsink. For a reference of the variants available refer to the RGx1..N datasheets. There are 2 variants of the RGx1..N, the RGx1A..N is the zero cross relay including various switching modes such as ON/OFF, Burst, Distributed full cycle and Advanced full cycle modes. The RGx1P..N is the proportional control variant which on top of the aforementioned switching modes includes also phase angle switching and soft starting features. The NRG family includes also 2-pole and 3-pole proportional control solid state relays RGC2/3P..N capable of switching loads in different configurations including start, delta, star with neutral, a 1-pole load between phases and 1-pole load between phase and neutral.

The RGx1A..D..N switching is controlled only via the control voltage at the A1, A2 control input terminals. Communication through the internal BUS is required for measurement and diagnostics data only.

The RG..CM..N utilises the communication system for switching, measurement and diagnostic thus minimising the number of components required in the system.

For more information on the functions of each variant refer to Section 6.

Through the internal BUS, the main controller can read measurements, parameters and diagnostics information related to the RG..N and its load. The RG..N is also capable of detecting certain fault conditions. A fault condition is indicated through a red LED available on the facade of the RG..N. The type of fault can be identified through a specific flash rate of the red LED and identified via the communication system.

Since the main controller needs to address each specific RG..N individually, each RG..N needs to be uniquely identifiable. It is not required to physically set the ID for each RG..N. This can be done through an auto-addressing function which occurs automatically on the first start up; whereby each RG..N on the bus chain will automatically be assigned an ID with respect to its physical placement on the internal bus.

NRG internal cables

The RCRGN-xxx-2 is a 5-way proprietary cable used for the internal BUS, i.e., between the NRG controller and the first RG..N on the BUS chain and between respective RG..Ns on the BUS. This internal BUS cable though terminated with a micro-USB plug is not a standard USB cable. Apart from the data and supply lines, the RCRGN-xxx-2 are equipped with an additional wire utilised for the auto-addressing of the RG..Ns on the NRG bus chain. These cables are available in various lengths from Carlo Gavazzi.



For further technical information on each NRG system component please refer to the respective product datasheets:

System component	Datasheet	QR code
NRGC	https://www.gavazziautomation.com/fileadmin/images/PIM/DATASHEET/ENG/SSR_NRGC.pdf	
RGx1A..D..N	https://www.gavazziautomation.com/fileadmin/images/PIM/DATASHEET/ENG/SSR_RG_D_N.pdf	
RGx1..CM..N	https://www.gavazziautomation.com/fileadmin/images/PIM/DATASHEET/ENG/SSR_RG_CM_N.pdf	
RGC2/3P..N	https://www.gavazziautomation.com/fileadmin/images/PIM/DATASHEET/ENG/SSR_RGC_2_3_N.pdf	
RCRGN-xxx-2	https://www.gavazziautomation.com/fileadmin/images/PIM/DATASHEET/ENG/SSR_Accessories.pdf	

3. Installation

EN

Installation general requirements

Avoid installing the device in environments with the following characteristics:

- relative humidity higher than 95% or with condensation;
- strong vibrations or shocks;
- exposure to water sprays;
- exposure to aggressive and polluting atmospheres (e.g.: sulphur and ammonia fumes, saline mist, smoke) to avoid corrosion and/or oxidation;
- strong magnetic and/or radio frequency interference (thus avoid installation near transmitting antennae);
- exposure of the devices to direct sunlight and the elements in general.

3.1. System configuration

The NRG bus chain can consist of 1 x NRG controller and either up to 48 x RGx1A..D..N SSRs or 32 x RGx1..CM..N SSRs. When 2-pole/3-pole NRG SSRs (RGC2/3P..N) are utilised, a maximum of 32 switched poles can be connected to each NRG controller. RGx1..CM..N and RGC2/3P..CM..N SSRs can be mixed on the same bus chain. The RGx1A..D..N SSRs cannot be mixed with any of the RG..CM..N SSRs on the same bus chain.

The NRG controller is the interface to the main controller, equipped with 2 x RJ45 ports to allow daisy chaining from one NRGC to another. A terminating resistor must be fitted at the end of the RS485 network, i.e. on the last NRGC in the system. The number of NRGCs in the system cannot exceed 247, with each NRGC identified by a unique Modbus ID. The NRGC ID can be set either manually via the hex switch under the door flap at the front of the device (refer to Section 6.1.1), or through Modbus using specific commands as explained in Section 6.1.2.

The connection between the NRG controller and the solid state relays is through the internal bus cables. Each RG..N is equipped with 2 x micro USB ports to allow looping between one RG..N and another using the RCRGN-xxx-2 bus cables from Carlo Gavazzi. The RGN-TERMRES supplied with each NRG controller has to be connected to the last RG..N on the NRG bus chain.

The NRG controller has to be supplied with a 24VDC supply via the supply input plug (Us-, Us+). Power to the RG..N SSRs on the bus chain is provided via the internal bus cables through the NRG controller.

The RGx1..N SSRs require a mains reference connection with respect to the load (neutral or another phase) through the 'Ref' connector to provide voltage and power measurements.
The Ref connector has 2 x internally shorted terminals to allow for looping of the mains reference onto various RG..Ns. Refer to the 'Load connection diagrams' section (Section 3.3) for more information. This is not applicable for RGC2/3P..N SSRs.

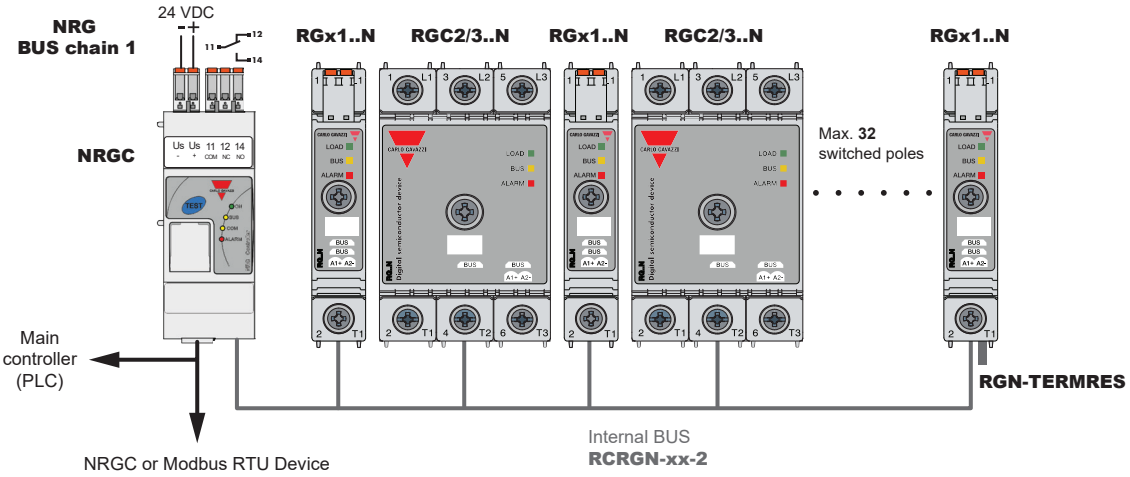


Fig. 2 - NRG bus chain configuration

3.2. Connection diagrams

The NRG bus chain can be connected in a line topology with a maximum of 247 NRGCs. The NRGC has two roles. It is the master of the BUS chain when the main controller requests the specific NRGC to perform actions on the solid state relays connected to its BUS chain, such as for example in the case of configuration and for status or diagnostic checks. In the cases where the main controller needs to address the solid state relays to get measurement parameters, the NRGC acts only as a byte repeater.

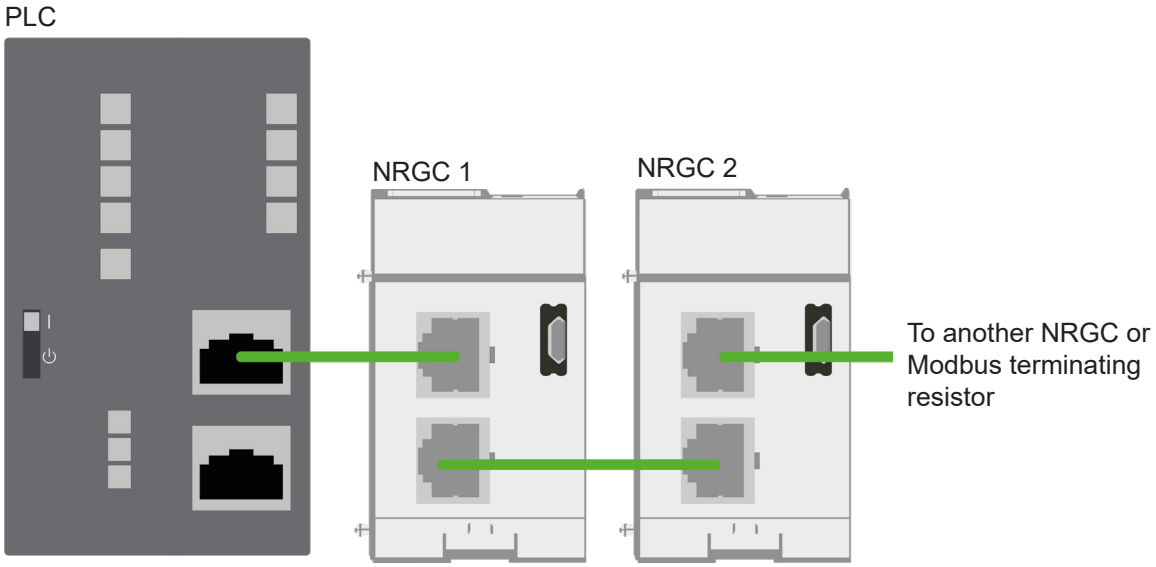


Fig. 3 - NRG bus chain connected in a line topology

3.3. Load connection diagrams

RGx1..N load connection diagrams

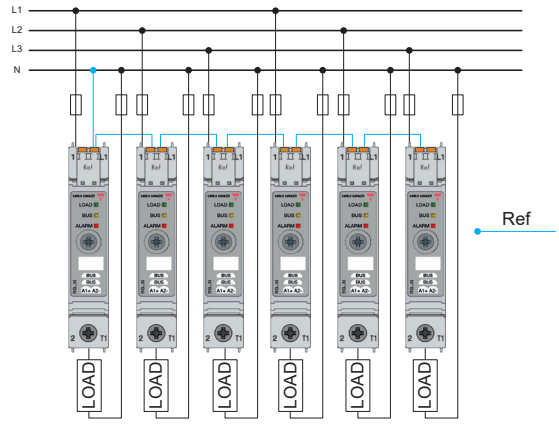


Fig. 4 - Loads connected between phase and neutral. The Ref connections can be looped from one RG..CM..N to another since all the loads have the same return path

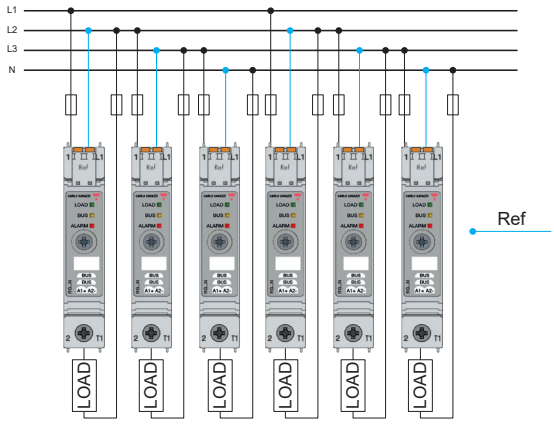


Fig. 5 - Loads connected between phases. Reference connection (Ref) should always follow the return path of the load

RGC2/3P..N load connection diagrams

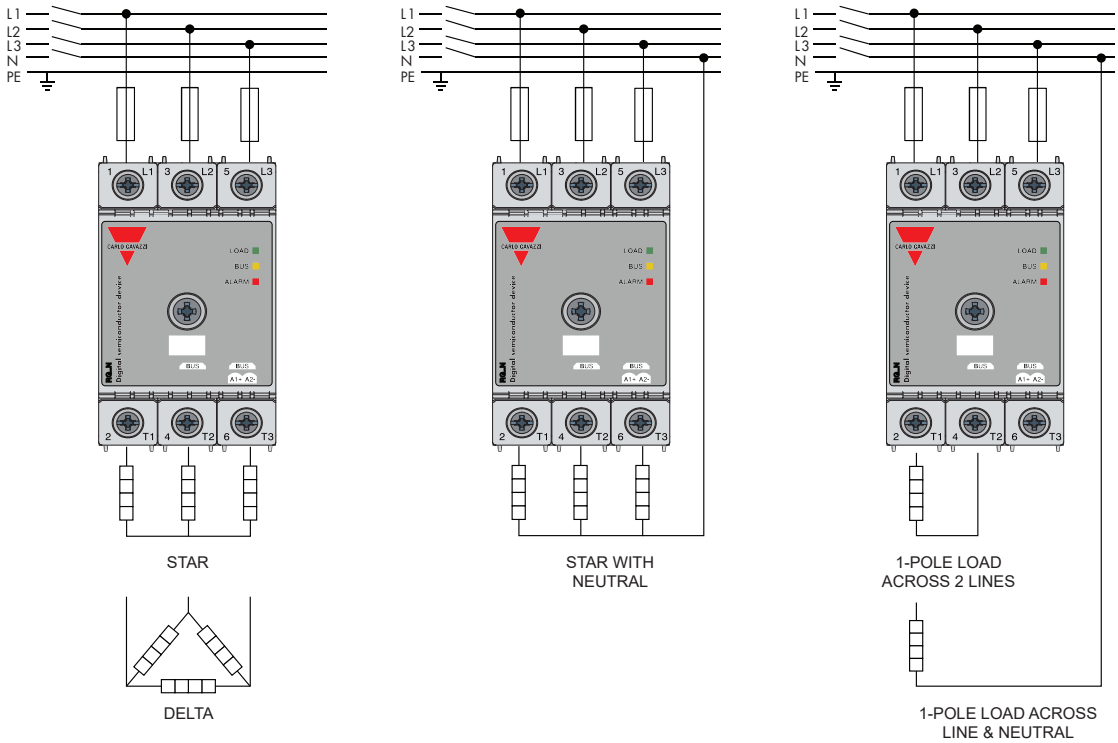


Fig. 6 - Possible load configurations for the RGC2/3P..N including star, delta, star with neutral, 1-pole load across L1- L2, 1-pole load across L2 - L3, 1-pole load across L1 - L3, 1-pole load across L1 - N, 1-pole load across L2 - N, and 1-pole load across L3 - N

3.4. AutoConfiguration

AutoConfiguration (AutoConfig) is used to automatically assign an ID to the RG..Ns on each BUS chain. AutoConfiguration is a command that is executed when the main controller sends this specific command request to the NRGC. Through this command, the NRGC permanently assigns an ID to the RG..Ns connected on its BUS chain based on their physical location on the BUS and the NRGC ID to which they are connected. This means that each RG..N in the NRG system is uniquely identifiable.

For example;
RG..N in physical location 2 on the BUS chain of NRGC with ID 5, will be identifiable with RG..N ID 2 and NRGC ID 5.

For RGx1A..D..N, the maximum number of devices is 48. For RG..CM..N, the maximum number of devices on the bus chain (n) depends on the number of switched poles (**32 max**) which derives from the mix of **RGx1..N (1 switched pole)**, **RGC2P..N (2 switched poles)** and **RGC3P..N (3 switched poles)** devices on the same bus chain.

The RG..Ns are shipped in an un-configured state and thus need to be configured on first power-up. The status of each RG..N is readable through the RG..N Configuration Data Register (DCDR**aa**, where **aa** is the ID of the specific RG..N). An RG..N can have the following status:

- **Correctly Configured:**
  The RG..N ID stored in the RG..N is within the allowed range (1-48 for RG..D..N and 1-32 for RG..CM..N) and matches with the physical location of the RG..N on the BUS. Additionally, the NRGC ID stored in the RG..N matches with the ID of the NRGC to which the RG..N is connected
- **Un-Configured:**
  The RG..N ID stored in the RG..N is 255 (factory default ID) or outside the allowed range and/or the NRGC ID stored in the RG..N is 255, 0, or 248-254
- **Wrongly Configured:**
  The RG..N ID and the NRGC ID of the specific RG..N do not meet the criteria to be considered Correctly Configured and do not meet the criteria to be considered Un-Configured



It is strongly recommended that before an AutoConfiguration is executed, a check of the system is done to ensure that all is in order before assigning a permanent ID to the RG..Ns. These checks can be done through a Sequence or Presence Roll Call command. Following these commands, the counters of total number of end-devices (TPRDC), Correctly Configured device counter (CCFDC), Wrongly Configured Device Counter (WCFDC) and Un-configured Device Counter (UCFDC) are updated with the information retrieved from the system.

Further details are available in Section 6.3.

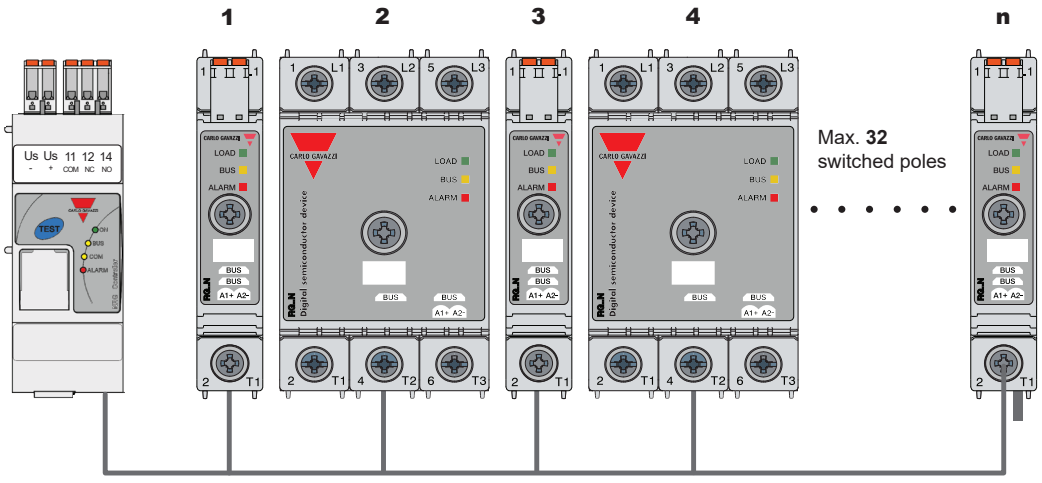


Fig. 7 - SSRs in NRG bus chain are automatically addressed based on their position on the bus

3.5. Grounding

Connecting the protective earth for the NRG solid state relays

The heatsink of the RGC..Ns has to be earthed. This can be done either via the metal DIN clip if the DIN rail is earthed, or through the connection provided using an M5 screw. Note that the M5 Protective Earth (PE) screw is not provided with the RG..N.

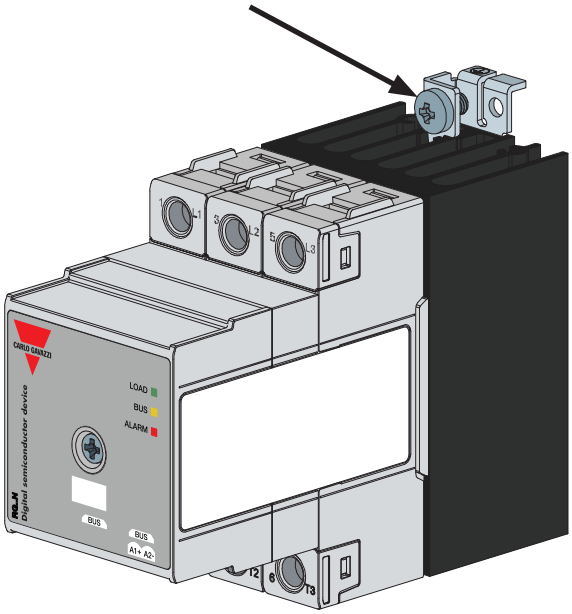


Fig. 8 - RG..N connection for Protective Earth (PE)

4. The Communication Interface

4.1. Mode of Operation

The RG..N is equipped with on-board communications to provide real time data of measured parameters and device status. The RG..CM..N variant of NRG solid state relay also has switching functions integrated through the communication. In this case, the RG..Ns need to be connected to an NRGC with the internal BUS cables, RCRGN-xxx-2.

The NRGC is in turn connected to the main controller or PLC via an RS485 interface. The communication protocol to communicate with the NRGC and hence the RG..Ns is Modbus RTU.

In order to enable communication, the communication settings of the main controller need to match the default communication settings of the NRGC. In case these do not match, the NRGC communication settings may be changed as explained in Section 6.2.

Each NRGC in the system need to be identifiable and so, each NRGC should have its ID set before operation can start (refer to Section 6.1 for NRGC Modbus ID settings and Section 4.8 for the message structure). The NRGC needs to be powered with a 24 VDC supply. Communication with RG..Ns can be carried out only if the RG..Ns are correctly configured (i.e., have a valid ID). Brand new units are shipped un-configured and need to be configured through an AutoConfig command at the very first power-up.

The NRG system provides flexibility in that some of the registers may have the default settings changed to be better suited for the needed application. The desired settings need to be communicated at every system power-up since the modified settings are not permanently stored. The tables below list the RG..N and NRGC registers and their default values after power reset. Details on the referred registers are explained in Section 5.

RGx1A..D..N

Holding Registers	Register		Register value after power reset
	OVLMR	Over voltage limit register	660
	UVLMR	Under voltage limit register	0
	OCLMR	Over current limit register	Model dependant
	UCLMR	Under current limit register	0
	OFLMR	Over frequency limit register	66
	UFLMR	Under frequency limit register	44
	OTPWR	Over-temperature warning	0
	CUHPR	Max. current period register	18

Input Registers	Register		Reading after power reset
	MCUR	Max. current register	Actual measurement
	VRRDR	Voltage reading register	Actual measurement
	FQRDR	Frequency reading register	Actual measurement
	CRRDR	Current reading register	Actual measurement
	APRDR	Apparent power reading register	Actual measurement
	RPRDR	Real power reading register	Actual measurement
	ENRDLR	Energy reading register	Reading at last power off
	ENRDHR	Energy reading register	
	OTRDR	On time reading register (running hours)	Reading at last power off

RGx1..CM..N

Holding Registers	Register		Register value after power reset
	LDOTWRR	Load Running hours Write Register	0
	EDCMDR	Command and Status Register	-
	LDVREFR	Load Deviation Voltage Ref Register	0
	LDIREFR	Load Deviation Current Ref Register	0
	LDEVPR	Load Deviation Percentage Register	10
	ALSTR	Alarm Setting Register	-
	OVLMR	Over Voltage Limit Register	660
	UVLMR	Under Voltage Limit Register	0
	OCLMR	Over Current Limit Register	Model dependant
	UCLMR	Under Current Limit Register	0
	OFLMR	Over Frequency Limit Register	66
	UFLMR	Under Frequency Limit Register	44
	OTPWR	Over Temperature Pre-Warning Register	0
	CUHPR	Max. Current Period Register	18
	OPSMR	Output Substitute Mode Register	1
	OPSVR	Output Substitute Value Register	0
	FMSTR	Switching Mode Setup Register	1
	TMBSR	Time Base Setting Register	0.1
	CTRLR	Control Level Register	0
	ONOF0R	ON/OFF 0 Control Register	0
	ONOF1R	ON/OFF 1 Control Register	0
	SSRTR	Soft start Ramping Time Register	0 *(only for RGx1P..CM..N)*
	SSOTR	Soft start OFF Time Register	5 *(only for RGx1P..CM..N)*
	SSCLR	Soft Start Current Limit Register	0 *(only for RGx1P..CM..N)*
	CVREFR	Voltage Compensation Reference Register	0 *(only for RGx1P..CM..N)*

Input Registers	Register		Register value after power reset
	AL1SR	Alarm 1 Status Register	-
	EDGSR	End-Device General Status Register	-
	CUHDR	Hold Current Reading Register	Actual measurement
	VRRDR	Voltage RMS Reading Register	Actual measurement
	FQRDR	Frequency Reading Register	Actual measurement
	CRRDR	Current RMS Reading Register	Actual measurement
	APRDR	Apparent Power Reading Register	Actual measurement
	RPRDR	Real Power Reading Register	Actual measurement
	ENRDLR	Energy Reading Low Register	Actual measurement
	ENRDHR	Energy Reading High Register	Actual measurement
	OTRDR	SSR Running Hours Read register	Last reading before power up
	LDOTRDR	Load Running Hours Read Register	1
	CTRLFBR	Control Feedback Register	0 *(only for RGx1P..CM..N)*

Holding Registers	Register		Register value after power reset
	LDOTWRR	Load Running hours Write Register	0
	EDCMDR	Command and Status Register	-
	LDVREF12R	Load Deviation Voltage Ref L1-L2 Register	0
	LDIREF1R	Load Deviation Current Ref L1 Register	0
	LDVREF23R	Load Deviation Voltage Ref L2-L3 Register	0
	LDIREF2R	Load Deviation Current Ref L2 Register	0
	LDVREF31R	Load Deviation Voltage Ref L3-L1 Register	0
	LDIREF3R	Load Deviation Current Ref L3 Register	0
	LDEVPR	Load Deviation Percentage Register	10
	ALSTR	Alarm Setting Register	-
	OVLMR	Over Voltage Limit Register	660
	UVLMR	Under Voltage Limit Register	0
	OCLM1R	Over Current Limit on L1 Register	Model dependant
	UCLM1R	Under Current Limit on L1 Register	0
	OCLM2R	Over Current Limit on L2 Register	Model dependant
	UCLM2R	Under Current Limit on L2 Register	0
	OCLM3R	Over Current Limit on L3 Register	Model dependant
	UCLM3R	Under Current Limit on L3 Register	0
	OFLMR	Over Frequency Limit Register	66
	UFLMR	Under Frequency Limit Register	44
	OTPWR	Over Temperature Pre-Warning Register	0
	CUHPR	Max. Current Period Register	18
	SSRTR	Soft start Ramping Time Register	0 *(only for RGC3P..N)*
	SSOTR	Soft start OFF Time Register	5 *(only for RGC3P..N)*
	SSCLR	Soft Start Current Limit Register	0 *(only for RGC3P..N)*
	LDCNCFR	Load Connection Configuration Register	0
	OPSMR	Output Substitute Mode Register	1
	OPSVR	Output Substitute Value Register	0
	FMSTR	Switching Mode Setup Register	1
	TMBSR	Time Base Setting Register	0.1
	CVREFR	Voltage Compensation Reference Register	0
	TPREFR	True Power Compensation Ref Power Register	0
	CTRLR	Control Level Register	0
	ONOF0R	ON/OFF 0 Control Register	0
	ONOF1R	ON/OFF 1 Control Register	0

Input Registers	Register		Register value after power reset
	CTRLFBR	Control Feedback Register	0
	AL1SR	Alarm 1 Status Register	-
	EDGSR	End-Device General Status Register	-
	VR12RDR	Voltage RMS L1-L2 Reading Register	Actual measurement
	VR23RDR	Voltage RMS L2-L3 Reading Register	Actual measurement
	VR31RDR	Voltage RMS L3-L1 Reading Register	Actual measurement
	CR1RDR	Current RMS L1 Reading Register	Actual measurement
	CR2RDR	Current RMS L2 Reading Register	Actual measurement
	CR3RDR	Current RMS L3 Reading Register	Actual measurement
	CUH1DR	Hold Current L1 Reading Register	Actual measurement
	CUH2DR	Hold Current L2 Reading Register	Actual measurement
	CUH3DR	Hold Current L3 Reading Register	Actual measurement
	RPRDR	Real Power Reading Register	Actual measurement
	APRDR	Apparent Power Reading Register	Actual measurement
	FQRDR	Frequency Reading Register	Actual measurement
	ENRDLR	Energy Reading Low Register	Actual measurement
	ENRDHR	Energy Reading High Register	Actual measurement
	OTRDR	SSR Running Hours Read register	Last reading before power up
	LDOTRDR	Load Running Hours Read Register	0

NRGC

Holding Registers	Register		Register value after power reset
	RLYCR	Relay configuration register	RLFNB = 1 Configured as Alarm EMR with none of the errors (Internal error, COM error, BUS error, Device limit / mismatch error, Termination error) masked
Input Registers	**Register**		**Reading after power reset**
	CTRSR	Controller (NRGC) status register	CRSTF Controller Reset Flag = 1
	LTOPR	Last operation register	0
	MBIDR	Modbus ID register	Stored value at power up
	MBBRR	Modbus BaudRate register	Stored value at power up
	MBPRR	Modbus parity register	Stored value at power up
	TPRDC	Total present device counter	0
	CCFDC	Correctly configured device counter	0
	WCFDC	Wrongly configured device counter	0
	UCFDC	Un-configured device counter	0
	EDIDRaa	RG..Nxx ID register for RG..Nxx	0
	CNIDRaa	NRGC ID register for RG..Nxx	0
	DCDRaa	RG..N configuration register for RG..Nxx	0
	DTY1Raa	Device type 1 register for RG..Nxx	0
	DTY2Raa	Device type 2 register for RG..Nxx	0
	SIN1aa	SIN 1 register for RG..Nxx	0
	SIN2aa	SIN 2 register for RG..Nxx	0

When the RG..Ns are configured and communication with the RG..Ns is possible, the main controller can read real time data and diagnostic information from the RG..N accessible registers.

Configuration data related to the RG..Ns, such as configuration status, device type, RG..N ID and NRGC ID of the respective RG..N, etc., is accessible only through the NRGC input registers. These registers are updated only after a Sequence Roll Call, a Presence Roll Call or an AutoConfig operation. Data from these registers is very useful for troubleshooting. Troubleshooting guides are provided in Chapter 7 of this document.

The real time data that can be accessed from each RGx1..N includes:

- RMS current in A – refer to Current Reading Register CRRDR
- Hold current in A – refer to Hold Current Register CUHDR
- RMS voltage in V – refer to Voltage Reading Register VRRDR
- Frequency in Hz – refer to Frequency Reading Register FQRDR
- Apparent Power in VA – refer to Apparent Power Reading Register APRDR
- Real Power in W – refer to Real Power Reading Register RPRDR
- Active Energy in kWh – refer to Energy Reading Register ENRDHR, ENRDLR
- Running hours (On Time) – refer to SSR Running hours Reading Register OTRDR

The real time data that can be accessed from each RGC2/3P..N includes:

- L1 RMS current in A – refer to L1 Current Reading Registers CR1RDR
- L2 RMS current in A – refer to L2 Current Reading Registers CR2RDR
- L3 RMS current in A – refer to L3 Current Reading Registers CR3RDR
- L1 Hold current in A – refer to L1 Hold Current Registers VR12RDR
- L2 Hold current in A – refer to L2 Hold Current Registers VR23RDR
- L3 Hold current in A – refer to L3 Hold Current Registers VR31RDR
- L1-L2 RMS voltage in V – refer to L1 Voltage Reading Registers CUH1DR
- L2-L3 RMS voltage in V – refer to L2 Voltage Reading Registers CUH2DR
- L3-L1 RMS voltage in V – refer to L3 Voltage Reading Registers CUH3DR
- Frequency in Hz – refer to Frequency Reading Register FQRDR
- Apparent Power in VA – refer to Apparent Power Reading Register APRDR
- Real Power in W – refer to Real Power Reading Register RPRDR
- Active Energy in kWh – refer to Energy Reading Register ENRDHR, ENRDLR
- SSR running hours – refer to SSR Running hours Reading Register OTRDR
- Load running hours – refer to Load Running hours Reading Register LDOTRDR

The End-device general status register **EDGSR** can be accessed to analyse the status of each RG..N. If all flags are clear it means that status of the specific RG..N is OK. If any of the error flags is set, one of the following alarm conditions has been identified:

- SSR over-temperature
- Mains loss
- Load loss / SSR open circuit
- SSR short circuit
- Frequency out of range
- Current out of range
- Voltage out of range
- Communication (BUS) error
- Internal error

The NRGC is subject to different failure modes than the RG..N. Status of the NRGC can be read from the Controller Status Register **CTRSR**. If all error flags are clear it means that status of the specific NRGC is OK. If any of the error flags is set, one of the following alarm conditions has been identified:

- Configuration error (Device limit or device mismatch error)
- BUS communication error
- COM communication error
- Internal error
- Termination BUS error

When an alarm condition is identified, apart from the flag in the respective register, the respective red ALARM LED on the RG..N and/or the NRGC is flashing ON with a specific flash rate to indicate the type of alarm identified. In the case of the NRGC and alarm errors related to the NRGC, the auxiliary EMR will function as an alarm EMR unless configured otherwise.

4.2. The data interface

The communication protocol adopted between the main controller and the NRGC(s) is the Modbus RTU, implemented according to published official Modbus documentation on www.modbus.org:

“Modbus Application Protocol Specification V1.1b3”
“Modbus over Serial Line Specification and Implementation Guide V1.12”

The communication link between the NRGC(s) and the main controller is based on an RS-485 physical layer using a 2-wire system. Hence the system will work in a half-duplex mode meaning that transmission of messages and replies cannot occur simultaneously.

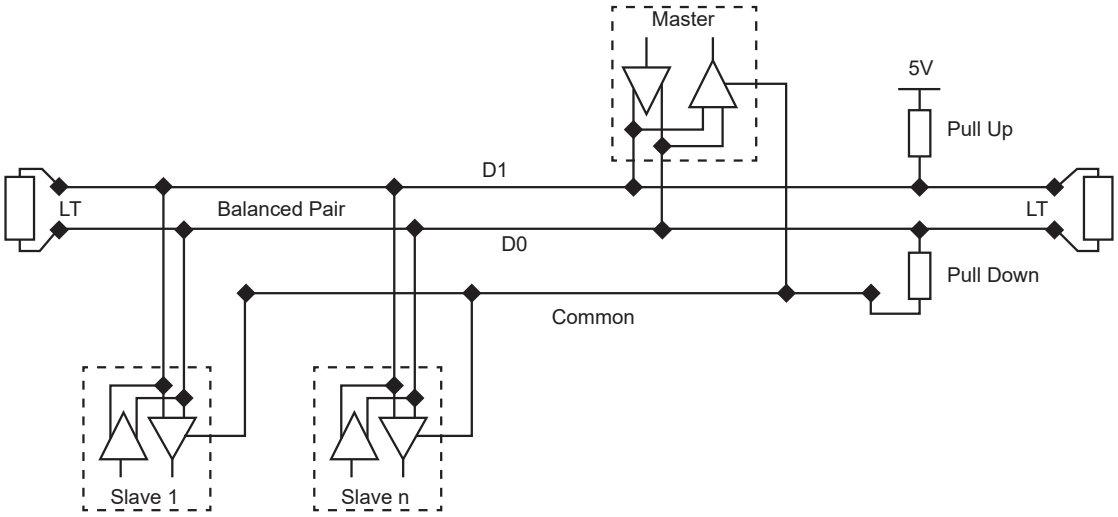


Fig. 9 - 2-wire topology

4.3. Communication cables

Use of shielded CAT-5e cables is recommended for the connection between the main controller and the NRGC and between other NRGC controllers. Cable colour-coding conforms to the TIA/EIA-568-B standard.

If using ready-made cables, verify that a straight cable is used. The cable shield must be connected to system ground at one end only. This is usually convenient to do at the side of the master device, i.e., the main controller or PLC.

The communication cable for the BUS chain between the NRGC and respective RG..Ns shall be the RCRGN-xxx-2.

4.4. Connector pin-out of RJ45 for 2-wire Modbus

The RJ45 physical connections shall be wired according to Figure 10 and table hereunder:

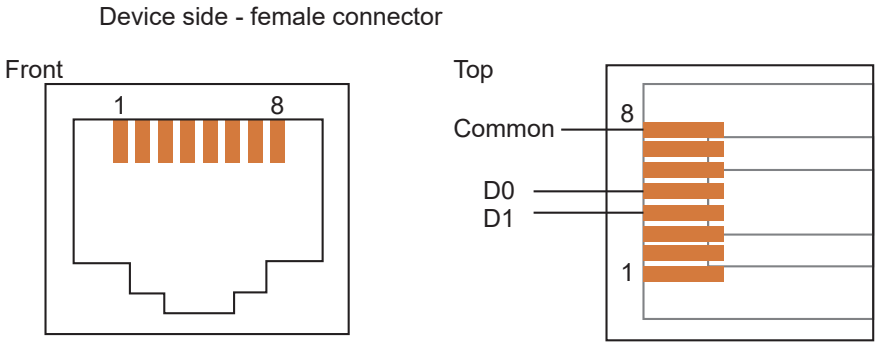


Fig. 10 - Required pin-out for 2-wire Modbus on RJ45 connector

Pin on RJ45	T568B Colour	Signal name	EIA-485 name	Description
1	White/Orange	-	-	-
2	Orange	-	-	-
3	White/Green	-	-	-
4	Blue	D1	B/B'	Transceiver terminal 1, V1 Voltage (V1/V0 for binary 1 [OFF] state)
5	White/Blue	D0	A/A'	Transceiver terminal 0, V0 Voltage (V0/V1 for binary 0 [ON] state)
6	Green	-	-	-
7	White/Brown	-	-	-
8	Brown	Common	C/C'	Signal and Power Supply Common

4.5. Communication settings

Parameter	Default Value	Other settings
Device address (NRGC ID)	1	1-247
Baud Rate	115200 bits/s	9600, 19200, 38400, 57600, 115200 bits/s
Data Format - Parity	Even	None, Even, Odd
Data Format – Stop Bits	1	1 (for odd or even parity) 2 (for no parity)
Data Format – Data Bits	8 bits	-

Default values can be updated through the **STIDR** (Set ID Register), **STBRR** (Set Baud Rate Register) and **STPRR** (Set Parity Register) (refer to Section 6.2 for further details). The NRGC ID can alternatively be changed through the NRGC hex switch (located behind the front door flap) for Modbus ID 1-15.

4.6. Inter-frame delays

The delay between request and response frame per Modbus standard is defined as 3.5 character time for baud rates ≤ 19200 or a delay of 1.75ms for baud rates > 19200.

Since the NRGC acts as a byte-repeater to forward messages from the main controller to the RG..N and vice versa, an additional delay is introduced in the communication between the main controller and the RG..N. For this reason, the inter-frame delay needs to be adjusted as indicated below to ensure reliable communication:

- an additional delay of about 0.9ms at a baud rate of 9600
- an additional delay of about 0.55ms at a baud rate of 19200
- an additional delay of about 100us at a baud rate of 38400, 57600 and 115200

4.7. Modbus RTU function codes

4.7.1. NRGC Modbus Functions

The following Modbus functions are available for the NRGC:

- Read Input Registers — function code 0x04
- Read Holding Registers — function code 0x03
- Write Single (Holding) Register — function code 0x06
- Write Multiple (Holding) Register — function code 0x10

4.7.2. RG..N Modbus functions

A special function code shall be used when the registers noted in Section 5.3, Section 5.4, Section 5.5, and Section 5.6 related to the RG end-devices need to be accessed. The use of the special function code indicates that the message is directly aimed to an RG..N and not the NRGC. When addressing the RG..N devices, the ID of the NRGC to which the RG..N is connected shall be included in the message but the NRGC acts only as a byte-repeater when this special function code is used and will not reply to the message. The message is passed to the addressed RG..N that will reply to the received message.

- Special function code — function code 0x44

Auxiliary function codes to the special function code 0x44:

- Read Input Registers — function code 0x04
- Read Holding Registers — function code 0x03
- Write Single (Holding) Register — function code 0x06
- Write Multiple (Holding) Registers — function code 0x10

4.8. Structure of messages

4.8.1. Differences between NRGC and RG..N related messages

Message request/reply format when addressing the **NRGC**:

Field	Field name	Value
1	Modbus Slave ID	NRGC ID (1 to 247)
2	Function code	Request:0x03, 0x04, 0x06, 0x10 Reply: 0x03, 0x04, 0x06, 0x10 Exception: 0x83, 0x84, 0x86, 0x90
3	Data associated to the requested function code	
4	CRC-16	

Message request/reply format when addressing **RG..Ns:**

Field	Field name		Value	Length
1	Modbus Slave ID		NRGC ID (=1 to 247)	1 Byte
2	Function code		Request: 0x44 Reply: 0x44 Exception: 0xC4	1 Byte
3	Data associated to the special function code	RG..N ID	RG..N ID (=1 to 48)	1 Byte
4		Aux-function code	Request: 0x03, 0x04, 0x06, 0x10 Reply: 0x83, 0x84, 0x86, 0x90	1 Byte
5		Data according to the Aux-function code		N Bytes
6	CRC-16			2 Bytes

The MSB of the Aux-function code indicates whether the message is a request message to an RG..N or a reply message from an RG..N. The table below shows the combinations for the MSB status related to the special function code 0x44:

MSB of special function code	MSB of Aux-function code	Note
Clear	Clear	Message is a request from the main controller to an RG..N
Clear	Set (Aux-function code + 0x80)	Message is a reply sent from the RG..N to the main controller
Set (Special function code + 0x80)	Set (Aux-function code + 0x80)	Message is an exception reply sent from the RG..N to the main controller

If an ID of 0 is used, a broadcast message is sent to all NRGCs in the system. It is strongly suggested not to perform broadcast requests since when a broadcast message is sent, none of the NRGCs will reply and there is no feedback as to whether the operation was successful or not.

The table below describes the different fields for the two message formats:

Field	NRGC related message	RG..N related message
1	This is the ID of the NRGC being addressed or replying. The ID is set as described in Section 6.1.	This is the ID of the NRGC to which the RG..N being addressed or replying is connected.
2	This specifies the function requested from the NRGC being addressed or the function to which the NRGC addressed is replying. In case of an exception response the MSB is set and hence the exception response would be 0x80+ function code.	A special function code is used when the RG..Ns are being addressed or replying. In case of an exception response the MSB is set and hence the exception response would be 0x80+special function code.
3	The data in this field is related to the requested function code.	This is an additional field associated to the special function code. In this field the ID of the RG..N being addressed or replying is included.
4	As per Modbus standard the last 2 bytes of each message are the CRC-16 of all the bytes transmitted in the message.	This auxiliary function specifies the function requested from the RG..N being addressed. In the case that the message is a request the same function codes as per Standard Modbus are used. In the reply frame the MSB is set and hence the reply is 0x80+Aux-function code used in the request message. This serves to indicate that the message is a reply message from an RG..N.
5		The data in this field is related to the requested auxiliary function code.
6		As per Modbus standard the last 2 bytes of each message are the CRC-16 of all the bytes transmitted in the message.
Examples	Section 4.8.2	Section 4.8.3

4.8.2. Examples of NRGC related messages

Function Code 0x04 – Read NRGC Input Registers

Request frame:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x04	0x04	Request to read 02 input registers starting at address 0x0234 from NRGC with ID 0x01
Starting address	2 Bytes	0x0000 to 0xFFFF	0x0234	
Quantity of 16-bit Registers (N)	2 Bytes	0x0001 to 0x007D	0x0002	
CRC-16	2 Bytes			

Correct response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x04	0x04	Reply from NRGC with ID 0x01 with the register values. N = 2
Byte count	1 Byte	2*N	0x04	
Register values	N*2 Bytes		Values	
CRC-16	2 Bytes			

Error response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01		
Error code	1 Byte	0x84		
Exception code	1 Byte	01, 02, 03 or 04		
CRC-16	2 Bytes			

Example:
Need to know the no. of RG..Ns and how many are correctly configured, unconfigured or wrongly configured, connected to BUS chain with NRGC having ID 5 (0x05).

Details of registers location and description is noted in Section 5.
The relevant counters to retrieve the needed information are:
TPRDC (Total Present Device Counter) in register location 0x0102
CCFDC (Correctly Configured Device Counter) in register location 0x0103
WCFDC (Wrongly Configured Device Counter) in register location 0x0104
UCFDC (Un-Configured Device Counter) in register location 0x0105

Request: 0x05 0x04 0x01 0x02 0x00 0x04 CRCL CRCH

Response: 0x05 0x04 0x08 0x00 0x0A 0x00 0x0A 0x00 0x00 0x00 0x00 CRCL CRCH
i.e., **TPRDC** = 10, **CCFDC** = 10, **WCFDC** = 0, **UCFDC** = 0
10 RG..Ns found on BUS chain of NRGC with ID 5 and all 10 RG..Ns are correctly configured.

Response: 0x05 0x04 0x08 0x00 0x0A 0x00 0x09 0x00 0x00 0x00 0x01 CRCL CRCH
i.e., **TPRDC** = 10, **CCFDC** = 9, **WCFDC** = 0, **UCFDC** = 1
10 RG..Ns found on BUS chain of NRGC with ID 5; 9 RG..Ns are correctly configured, 1 RG..N is unconfigured.

Function Code 0x03 – Read NRGC Holding Registers

Request frame:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x03	0x03	Request to read 02 holding registers starting at address 0x0150 from NRGC with ID 0x01
Starting address	2 Bytes	0x0000 to 0xFFFF	0x0150	
Quantity of 16-bit registers (N)	2 Bytes	0x0001 to 0x007D	0x0002	
CRC-16	2 Bytes			

Correct response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x03	0x03	Reply from NRGC with ID 0x01 with the register values. N = 2
Byte count	2 Bytes	2*N	0x04	
Register values	N* 2 Bytes		Values	
CRC-16	2 Bytes			

Error response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01	0x01	
Error code	1 Byte	0x083	0x03	
Exception code	1 Byte	01, 02, 03 or 04	0x04	
CRC-16	2 Bytes			

Function Code 0x06 – Write NRGC Single Register

Request frame:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x06	0x06	Request to write 0x0020 in holding register located at address 0x0236 of NRGC with ID 0x01
Register address	2 Bytes	0x0000 to 0xFFFF	0x0236	
Register value	2 Bytes	0x0000 to 0xFFFF	0x0020	
CRC-16	2 Bytes			

Correct response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x06	0x06	Reply from NRGC with ID 0x01 with register value 0x0020 written at address 0x0236
Register address	2 Bytes	0x0000 to 0xFFFF	0x0236	
Register value	2 Bytes	0x0000 to 0xFFFF	0x0020	
CRC-16	2 Bytes			

Error response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01		
Error code	1 Byte	0x86		
Exception code	1 Byte	01, 02, 03 or 04		
CRC-16	2 Bytes			

Example:
To configure the auxiliary EMR of the NRGC with ID 5 (0x05) as a general purpose EMR and activate this output.

The reference register in this case is the **RLYCR** (Relay Configuration Register) located at address 16 (0x10). Details related to this register are referred to in Section 5.2.1.

The **RLOSB** (Relay Output State Bit) shall be 1 to activate the EMR.
The **RLFNB** (Relay Function Bit) shall be 0 to have relay configured as a general purpose EMR
All other bits can be 0 or 1.
Hence, the following is to be noted in this register:
0000 0000 1111 1101
0x00FD

Request: 0x05 0x06 0x00 0x10 0x00 0xFD CRCL CRCH

Response: 0x05 0x06 0x00 0x10 0x00 0xFD CRCL CRCH
i.e. Auxiliary EMR set as a general purpose relay and was made to change state.

Function Code 0x10 – Write NRGC Multiple Registers

Request frame:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x10	0x10	Request to write the provided values in 5 holding registers starting at address 0x0240 of NRGC with ID 0x01
Starting address	2 Bytes	0x0000 to 0xFFFF	0x0240	
Quantity of 16-bit registers (N)	2 Bytes	0x0001 to 0x007B	0x0005	
Byte count	1 Byte	2*N	0x000A	
Register values	N*2 Bytes		Values	
CRC-16	2 Bytes			

Correct response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01 to 0xF7	0x01	NRGC with ID = 1
Function code	1 Byte	0x10	0x10	Reply from NRGC with ID 0x01 that 5 registers were written starting at address 0x0240
Starting address	2 Bytes	0x0000 to 0xFFFF	0x0240	
Quantity of 16-bit registers (N)	2 Bytes	0x0001 to 0x007B	0x0005	
CRC-16	2 Bytes			

Error response:

Description	Length	Value	Example	Note
Physical address (NRGC ID)	1 Byte	0x01		
Error code	1 Byte	0x90		
Exception code	1 Byte	01, 02, 03 or 04		
CRC-16	2 Byte			

4.8.3. Examples of RG..N related messages

Function Code 0x44, Aux-Function code 0x04 – Read RG..N Input Registers

A read operation cannot be requested in broadcast mode. Hence if the NRGC ID and/or the RG..N are set to 0 (broadcast) in a message, the message shall be ignored by all RG..N and no reply is sent back.

Request frame:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Request to read 06 input registers starting at address 0x0234 from RG..N no. 9 connected to NRGC with ID 0x05.
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x04	0x04	
Starting Address – Hi	2 Bytes	0x0000 to 0xFFFF	0x02	
Starting Address – Lo			0x34	
Quantity of 16-bit Registers (N) – Hi	2 Bytes	0x0001 to 0x007C	0x00	
Quantity of 16-bit Registers (N) – Lo			0x06	
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Correct response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Reply from RG..N no. 9 connected with NRGC with ID 0x05 with the register values
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x84	0x84 (0x04+0x80)	
Byte Count	1 Byte	2*N	12	
Register Values – Hi	N*2 Bytes	Each register value Hi Byte first		
Register Values – Lo				
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Error response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Exception reply 0xC4 from RG..N no. 9 connected with NRGC with ID 0x05
Function code	1 Byte	0xC4	0xC4 (0x44+0x80)	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x84	0x84 (0x04+0x80)	
Exception code	1 Byte	01, 02, 03, or 04		
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Example:
The main controller needs to read the hold current and voltage from RG in position 5 on the BUS chain of NRGC with ID 2 (0x02).

The reference registers in this case are the **APRDR** (Apparent Power Reading Register) and **FQRDR** (Frequency Reading Register) located at addresses 18 (0x12) and 19 (0x13) respectively.
Details related to these registers are referred to in Section 5.3, Section 5.4, Section 5.5, and Section 5.6.

Request: 0x02 0x44 0x05 0x04 0x00 0x12 0x00 0x02 CRCL CRCH

Response: 0x02 0x44 0x05 0x84 0x04 0x03 0xE8 0x00 0xE6 CRCL CRCH
Readings from RG..N in position 5 of BUS chain related to NRGC with ID 2 are:
Hold current = 0x03E8 = 1000 in resolution of 1 = 1000 VA
RMS voltage = 0x138A = 5002 in resolution of 0.01 = 50.02 Hz

Function Code 0x44, Aux-Function code 0x03 – Read RG..N Holding Registers

A read operation cannot be requested in broadcast mode. Hence if the NRGC ID and/or the RG..N are set to 0 (broadcast) in a message, the message shall be ignored by all RG..N and no reply is sent back.

Request frame:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Request to read 06 holding registers starting at address 0x0234 from RG..N no. 9 connected to NRGC with ID 0x05.
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x03	0x03	
Starting Address – Hi	2 Bytes	0x0000 to 0xFFFF	0x02	
Starting Address – Lo			0x34	
Quantity of 16-bit Registers (N) – Hi	2 Bytes	0x0001 to 0x007C	0x00	
Quantity of 16-bit Registers (N) – Lo			0x06	
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Correct response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Reply from RG..N no. 9 connected with NRGC with ID 0x05 with the register values
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x83	0x83 (0x03+0x80)	
Byte Count	1 Byte	2*N	12	
Register Values – Hi	N*2 Bytes	Each register value Hi Byte first		
Register Values – Lo				
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Error response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Exception reply 0xC4 from RG..N no. 9 connected with NRGC with ID 0x 05
Function code	1 Byte	0xC4	0xC4 (0x44+0x80)	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x83	0x83 (0x03+0x80)	
Exception code	1 Byte	01, 02, 03, or 04		
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Broadcast for Aux-Function codes 0x06 and 0x10 with Function code 0x44

These are write commands and so it is possible to perform such commands in broadcast form. This should be done with great caution. Since a message contains both the NRGC ID and the RG..N ID, several possibilities of broadcast forms exist:

- In request message - NRGC ID = 0 & RG..N ID = 0.
  The write command will apply to all RG..Ns present in the NRG hierarchy since all RG..Ns connected to all NRGCs are being addressed.

- In request message - NRGC ID = 0 & RG..N ID = IDxx
  The write command will apply to the particular RG..N having the specified IDxx that may be present in any of the BUS chains connected to all NRGCs present in the system.

- In request message - NRGC ID = IDxx & RG..N ID = 0
  The write command will apply to all RG..Ns connected to the particular NRGC (NRGC xx) being addressed.

In all of the above cases, none of the RG..Ns will reply to the request.

Function Code 0x44, Aux-Function code 0x06 – Write RG..N Single Register

Request frame:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Request to write 0x1146 in holding register located at address 0x0234 of RG..N no. 9 connected to NRGC with ID 0x05
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x06	0x06	
Register Address – Hi	2 Bytes	0x0000 to 0xFFFF	0x02	
Register Address – Lo			0x34	
Register value – Hi	2 Bytes	0x0000 to 0xFFFF	0x11	
Register value – Lo			0x46	
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Correct response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Reply from RG..N no. 9 connected with NRGC with ID 0x05 with the register value 0x1146 written at address 0x0234
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x86	0x86 (0x06+0x80)	
Register Address – Hi	2 Bytes	0x0000 to 0xFFFF	0x02	
Register Address – Lo			0x34	
Register Values – Hi	2 Bytes	0x0000 to 0xFFFF	0x11	
Register Values – Lo			0x46	
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Error response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Exception reply 0xC4 from RG..N no. 9 connected with NRGC with ID 0x05
Function code	1 Byte	0xC4	0xC4 (0x44+0x80)	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x86	0x86 (0x06+0x80)	
Exception code	1 Byte	01, 02, 03, or 04		
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Function Code 0x44, Aux-Function Code 0x10 – Write RG..N Multiple Registers

Request frame:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Request to write provided values in 6 holding registers starting at address 0x0234 of RG..N no. 9 connected to NRGC with ID 0x05
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x10	0x10	
Starting Address - Hi	2 Bytes	0x0000 to 0xFFFF	0x02	
Starting Address - Lo			0x34	
Quantity of 16-bit Registers (N) – Hi	2 Bytes	0x0001 to 0x007A	0x00	
Quantity of 16-bit Registers (N) – Lo			0x06	
Byte Count	1 Byte	2* N	12	
Register Value - Hi	N*2 Bytes	Each register value, Hi Byte first	Value	
Register Value - Low				
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Correct response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Reply from RG..N no. 9 connected with NRGC with ID 0x05 on the qty. of registers written and the starting address
Function code	1 Byte	0x44	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x90	0x90 (0x10+0x80)	
Starting Address – Hi	2 Bytes	0x0000 to 0xFFFF	0x02	
Starting Address – Lo			0x34	
Quantity of 16-bit Registers (N) – Hi	2 Bytes	0x0001 to 0x007A	0x00	
Quantity of 16-bit Registers (N) – Lo			0x06	
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

Error response:

Description	Length	Value	Example	Note
Physical Address (NRGC ID)	1 Byte	0x01 to 0xF7	0x05	Exception reply 0xC4 from RG..N no. 9 connected with NRGC with ID 0x05
Function code	1 Byte	0xC4	0x44	
RG..N ID	1 Byte	0x01 to 0x30	0x09	
Aux-function code	1 Byte	0x90	0x90 (0x10+0x80)	
Exception code	1 Byte	01, 02, 03, or 04	0x00	
CRC-16 – Lo	2 Bytes			
CRC-16 – Hi				

4.9. Message handling strategy

- If a read/write request is sent to the NRGC whilst the NRGC is busy performing an operation with the RG..Ns (Controller Busy Flag, **CTRBF**, is set), the request will be rejected (except for limited access as explained in Section 5.2.2 for the NRGC Status Register) using error code 06 meaning that the device is currently busy and cannot provide the required data.
- If a request is sent to the NRGC to initiate an operation with the RG..Ns (using the CMMDB bits) and this request is accepted by the NRGC, the NRGC will reply back with an exception response using error code 5 indicating that the request was acknowledged and the NRGC shall enter busy mode to execute the requested command.

In the NRG system, the NRGC is sometimes acting as a byte-repeater to let through messages from the main controller to the RG..Ns. The below explains the function code handling strategy adopted to cover this scenario:

- If a message with an unused function code is sent to an NRGC, the NRGC addressed in the message will reject the message with an exception response with error code 01 (unknown function code).
- If a message with an unused special function code (65-72 and 100-110) is sent, neither the NRGC nor the RG..N accept and reply to this message and hence a timeout will occur.
- If a special function code is used in a message but a wrong or unused Aux-Function code is specified, the respective device will reply back with an exception response with error code 01 (unknown function code).

The Modbus standard clearly indicates the rules for message structure but does not define the expected behaviour if messages not as expected are received/transmitted. The following strategy was adopted:

- If a message exceeds 256 bytes, the message will be all discarded including the remaining incoming bytes in excess of 256 bytes. The respective device will go back to idle mode.
- If a message received is less than 4 bytes, the message is ignored and the NRGC goes back to idle mode.
- If the data provided in a message associated with a particular function code is not as expected for certain conditions an exception response with code 04 is issued. For example, if in a write command, more (or less) data values are provided than expected. In this case, the message is ambiguous and hence is not accepted.
- If the message length of a received message is not as expected, indicating that the content of the message is ambiguous, the message is rejected with error code 04.
- In the case that multiple registers are written in one operation and one of the registers being written in this message contains an illegal value intended for that particular register, the entire message will be discarded and none of the registers will be updated (including those registers in the message that contained correct values).

5. Registers

5.1. NRGC Register Map

NRGC Holding Registers

Category	Reference	Description	Location	Location (Hex)
Commands	**CMDSTR**	Command and Setup Register	1	0001
Configuration	**RLYCR**	Relay Configuration Register	16	0010
Communication Parameters	**STIDR**	Set ID Register	64	0040
	STBRR	Set BaudRate Register	65	0041
	STPRR	Set Parity Register	66	0042

NRGC Input Registers

Category	Reference	Description	Location	Location (Hex)
Status	**CTRSR**	NRGC (Controller) Status Register	256	0100
	LTOPR	Last Operation Register	257	0101
Communication Parameters	**MBIDR**	Modbus ID Register	272	0110
	MBBRR	Modbus BaudRate Register	273	0111
	MBPRR	Modbus Parity Register	274	0112
RG..N configuration data	**TPRDC**	Total Present Device Counter	258	0102
	CCFDC	Correctly Configured Device Counter	259	0103
	WCFDC	Wrongly Configured Device Counter	260	0104
	UCFDC	Un-Configured Device Counter	261	0105
	EDIDR01	End Device (RG..N) ID Register 01	288	0120
	EDIDRaa	End Device (RG..N) ID Register aa (where aa = 02 to 47)	289 - 334	0121 - 014E
	EDIDR48	End Device (RG..N) ID Register 48	335	014F
	CNIDR01	NRGC ID Register 01	352	0160
	CNIDRaa	NRGC ID Register aa (where aa = 02 to 47)	353 - 398	0161 - 018E
	CNIDR48	NRGC ID Register 48	399	018F
	DCDR01	Device Configuration Data Register 01	416	01A0
	DCDRaa	Device Configuration Data Register aa (where aa = 02 to 47)	417 - 462	01A1 - 01CE
	DCDR48	Device Configuration Data Register 48	463	01CF
	DTY1R01	Device Type 1 Register 01	480	01E0
	DTY2R01	Device Type 2 Register 01	481	01E1
	DTY1Raa	Device Type 1 Register aa (where aa = 02 to 47)	482 - 573	01E2 - 023D
	DTY2Raa	Device Type 2 Register aa (where aa = 02 to 47)		
	DTY1R48	Device Type 1 Register 48	574	023E
	DTY2R48	Device Type 2 Register 48	575	023F
	SIN1R01	SIN-address 1 Register 01	608	0260
	SIN2R01	SIN-address 2 Register 01	609	0261
	SIN1Raa	SIN-address 1 Register aa (where aa = 02 to 47)	610 - 701	0262 - 02BD
	SIN2Raa	SIN-address 2 Register aa (where aa = 02 to 47)		
	SIN1R48	SIN-address 1 Register 48	702	02BE
	SIN2R48	SIN-address 2 Register 48	703	02BF

5.2. NRGC Registers Description

5.2.1. NRGC Holding Registers (Read/Write Access)

CMDSTR – Command and Status Register
Register location - 1 (0x0001)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CMMDB [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-7:
CMMDB – Command Bits
These bits hold the command that shall be executed by the NRGC. Writing the value of 0 has NO effect on this register and no command will be executed. This should be avoided as this will automatically remove the traceability of the last command that was executed.

Value	Mode	Description
0x0	No Effect (default value)	
0x1	Sequence Roll Call	The NRGC initiates a scan of the RG..Ns on the BUS chain and checks the correct Sequence of the RG..Ns positioning on the BUS chain. This is the only command that can detect if more RG..Ns than the max. allowed are connected to the BUS chain.
0x2	Presence Roll Call	The NRGC checks ONLY the Presence of the RG..Ns on the BUS chain (irrespective of their location). The Sequence Roll Call and Presence Roll Call use different mechanisms and hence results from these operations can differ. The Presence Roll Call is ideally preceded with a Sequence Roll Call operation.
0x3	AutoConfig	The NRG Controller assigns an ID to the RG..Ns based on their physical location on the BUS chain and the NRGC ID to which they are connected.
0x4	Communications Check Start	Initiates a check of the communications link between NRGC and RG..Ns. This is useful for fault diagnostics
0x5	Communications Check Stop	
0x6	Communication Settings Update	Updates communication settings from default settings to required settings.
0x7	Set Device Mismatch Alarm	Management of device mismatch alarm in case the no. of RG..Ns found on the BUS chain is less than expected.
0x8	Clear Device Mismatch Alarm	
0x9 - 0xFF	Reserved for future use	

Writing a valid command to the **CMMDB** when the NRGC is busy performing an operation (**CTRBF** in the **CTRSR** is set) will result in an exception response with exception code 6 and the value in the **CMMDB** bits will not be updated with the value that was attempted to be written. The only exception is writing a Communications Check Stop command when a Communications Check is currently on-going.

Writing a valid command to the **CMMDB** when the NRGC is not busy performing an operation (**CTRBF** in the **CTRSR** is clear) will result in the request being accepted. The value of the **CMMDB** bits will be updated to the new written value, the **CTRBF** in the **CTRSR** will be set to indicate that the NRGC is now busy performing the requested operation. When a valid command written to the **CMMDB** bits is accepted and as a result of this, the NRGC goes in busy mode, the NRGC shall reply back to the request with an exception response using exception code 5 – meaning that the NRGC has acknowledged the request but is now busy performing an operation.

Bits 8-15:
Not used. Although writing to these bits has no effect, it is strongly recommended to write only 0s in these bits.

RLYCR – Relay Configuration Register

Register location - 16 (0x0010)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									TMERF	DMERF	DLERF	BSERF	CMERF	INERF	RLFNB	RLOSB
Status after reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

The auxiliary EMR available on the NRGC is set as an Alarm relay by default, i.e., it operates in case an Alarm condition is present on the NRGC. However, it is possible to set this EMR as a general purpose relay. The mode of the EMR (i.e. general purpose or Alarm EMR) is defined by the **RFLNB** bit (Bit 1). When the EMR is set as a general purpose EMR, the function of the EMR is dictated by the state of the **RLOSB** bit (Bit 0).

Bit 0:
RLOSB – Relay Output State Bit
This bit indicates the state of the EMR – Normally Open (NO) or Normally Closed (NC) and is relevant only for when the **RLFNB** = 0. **RLFNB** = 0 means the EMR will act as a general purpose relay and its function is determined by the state of the **RLOSB**.

RLOSB = 0: the EMR is not activated.
COM terminal 11 of the EMR will be connected to the NC terminal 12 and the NO terminal 14 shall be open circuit (floating).
RLOSB = 1: the EMR is activated.
COM terminal 11 of the EMR will be connected to the NO terminal 14 and the NC terminal 12 shall be open circuit (floating).

Bit 1:
RLFNB – Relay Function Bit
This bit indicates the mode of the EMR present on the NRGC.
RLFNB = 0: EMR in general purpose mode and its state is controlled by the **RLOSB.**
RLFNB = 1: EMR in Alarm mode and its state is controlled by the alarm status of the NRGC.
The alarm conditions for the NRGC include: Internal error, COM error, BUS error, Device limit and Device mismatch and Termination error.

It is possible to select the type of alarm for which the EMR (when set as an Alarm EMR, **RLFNB** =1) is to be activated by bits 2 to 6 as explained below:

Bit 2:
INERF – Internal Error Flag
This bit acts as a mask bit for the Internal Error indicated by the **INERF** bit (bit 2) in the NRGC Status Register (**CTRSR**).
INERF = 0: the **INERF** bit in the NRGC Status Register (**CTRSR**) does not contribute to activate the NRGC EMR when **RLFNB** is set as Alarm EMR.
INERF = 1: the **INERF** bit in the NRGC Status Register (**CTRSR**) will contribute to activate the NRGC EMR.

Bit 3:
CMERF – COM Error Flag
This bit acts as a mask bit for the COM Error indicated by the **CMERF** bit (bit 3) in the NRGC Status Register (**CTRSR**).
CMERF = 0: the **CMERF** bit in the NRGC Status Register (**CTRSR**) does not contribute to activate the NRGC EMR.
CMERF = 1: the **CMERF** bit in the NRGC Status Register (**CTRSR**) will contribute to activate the NRGC EMR.

Bit 4:
BSERF – BUS Error Flag
This bit acts as a mask bit for the BUS Error indicated by the **BSERF** bit (bit 4) in the NRGC Status Register (**CTRSR**).
BSERF = 0: the **BSERF** bit in the NRGC Status Register (**CTRSR**) will not contribute to activate the NRGC EMR.
BSERF = 1: the **BSERF** bit in the NRGC Status Register (**CTRSR**) will contribute to activate the NRGC EMR.

Bit 5:
DLERF – Device Limit Error Flag
This bit acts as a mask bit for the Device Limit Error indicated by the **DLERF** bit (bit 5) in the NRGC Status Register (**CTRSR**).
DLERF = 0: the **DLERF** bit in the NRGC Status Register (**CTRSR**) will not contribute to activate the NRGC EMR.
DLERF = 1: the **DLERF** bit in the NRGC Status Register (**CTRSR**) will contribute to activate the NRGC EMR.

Bit 6:
DMERF – Device Mismatch Error Flag
This bit acts as a mask bit for the Device Mismatch Error indicated by the **DMERF** bit (bit 6) in the NRGC Status Register (**CTRSR**).
DMERF = 0: the **DMERF** bit in the NRGC Status Register (**CTRSR**) will not contribute to activate the NRGC EMR.
DMERF = 1: the **DMERF** bit in the NRGC Status Register (**CTRSR**) will contribute to activate the NRGC EMR.

Bit 7:
TMERF – Termination Error Flag
This bit acts as a mask bit for the Termination Error indicated by the **TMERF** bit (bit 7) in the NRGC Status Register (**CTRSR**).
TMERF =0: the **TMERF** bit in the NRGC Status Register (**CTRSR**) will not contribute to activate the NRGC EMR.
TMERF = 1: the **TMERF** bit in the NRGC Status Register (**CTRSR**) will contribute to activate the NRGC EMR.

Bits 8-15:
Not used. Although writing to these bits has no effect, it is strongly recommended to write only 0s in these bits.

If for example, it is desired to have the NRGC EMR function ONLY when an alarm condition of Device Limit is identified (**DLERF** in **CTRSR** set), the contents of the **RLYCR** shall read as follows:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									TMERF	DMERF	DLERF	BSERF	CMERF	INERF	RLFNB	RLOSB
Status after reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

The table below shows other conditions for the NRGC EMR status; x represents either 1 or 0:

Bits in **CTRSR** (actual Alarm Status of the NRGC)						Masking Bits in **RLYCR**						Mode set for NRGC EMR in **RLYCR**		Relay Status	Comments
TMERF	DMERF	DLERF	BSERF	CMERF	INERF	TMERF	DMERF	DLERF	BSERF	CMERF	INERF	RLFNB	RLOSB		
X	X	X	X	X	1	X	X	X	X	X	1	1	X	Activated	Alarm status = Internal Error EMR set as Alarm, INERF in RLYCR not masked
0	0	0	0	0	1	1	1	1	1	1	0	1	X	Not Activated	Alarm status = Internal Error EMR set as Alarm but INERF in RLYCR is masked
X	X	X	X	1	X	X	X	X	X	1	X	1	X	Activated	Alarm status = COM Error EMR set as Alarm, CMERF in RLYCR not masked
X	X	X	1	X	X	X	X	X	1	X	X	1	X	Activated	Alarm status = Bus Error EMR set as Alarm, BSERF in RLYCR not masked
X	X	1	X	X	X	X	X	1	X	X	X	1	X	Activated	Alarm status = Device Limit Error EMR set as Alarm, DLERF in RLYCR not masked
X	1	X	X	X	X	X	1	X	X	X	X	1	X	Activated	Alarm status = Device Mismatch Error EMR set as Alarm, DMERF in RLYCR not masked
1	X	X	X	X	X	1	X	X	X	X	X	1	X	Not Activated	Alarm status = Termination Error EMR set as Alarm, TMERF in RLYCR not masked
0	0	0	0	0	0	1	1	1	1	1	1	1	X	Not Activated	No Alarm condition
Any combination other than above												1	X	Not Activated	
X	X	X	X	X	X	X	X	X	X	X	X	0	0	Not Activated	EMR set as General Purpose and is not activated
X	X	X	X	X	X	X	X	X	X	X	X	0	1	Activated	EMR set as General Purpose and is activated

STIDR – Set ID Register

Register location - 64 (0x0040)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									STIDR [7:0]							
Status after reset	0	0	0	0	0	0	0	0	Refer to below							

Bits 0-7:

STIDR – Set ID Register

This register holds the Modbus ID to be set in the NRGC when a Communications Settings Update command is requested. At power-up the value of this register is set to the value of the **MBIDR** register. The allowed values that can be written in this register are the same as described for the **MBIDR** register. If an invalid value is attempted to be written in this register, the request will be rejected (exception response) and the contents of this register shall remain unchanged.

Bits 8-15:

Not used. Although writing to these bits has no effect, it is strongly recommended to write only 0s in these bits.

STBRR – Set BaudRate Register

Register location - 65 (0x0041)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													STBRR [3:0]			
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	Refer to below			

Bits 0-3:

STBRR – Set BaudRate Register

This register holds the Modbus BaudRate to be set in the NRGC when a Communications Settings Update command is requested. At power-up the value of this register is set to the value of the **MBBRR** register. The allowed values that can be written in this register are the same as described for the **MBBRR** register. If an invalid value is attempted to be written in this register, the request will be rejected (exception response) and the contents of this register shall remain unchanged.

Bits 4-15:

Not used. Although writing to these bits has no effect, it is strongly recommended to write only 0s in these bits.

STPRR – Set Parity Register

Register location - 66 (0x0042)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														STPRR [2:0]		
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	Refer to below		

Bits 0-2:

STPRR – Set Parity Register

This register holds the Modbus Parity to be set in the NRGC when a Communications Settings Update command is requested. At power-up the value of this register is set to the value of the **MBPRR** register. The allowed values that can be written in this register are the same as described for the **MBPRR** register. If an invalid value is attempted to be written in this register, the request will be rejected (exception response) and the contents of this register shall remain unchanged.

Bits 3-15:

Not used. Although writing to these bits has no effect, it is strongly recommended to write only 0s in these bits.

5.2.2. NRGC Input Registers (Read Access)

CTRSR – NRGC (Controller) Status Register
Register location - 256 (0x0100)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CTRBF	USBNF							TMERF	DMERF	DLERF	BSERF	CMERF	INERF		CRSTF
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit 0:
CRSTF – Controller Reset Flag
This is set every time the NRGC supply is re-setted. This bit is cleared to 0 once the CTRSR is read.

Bit 1:
Not used.

Bit 2:
INERF – Internal Error Alarm Flag
This flag is set in case of an internal error in the NRGC. This flag is cleared once the internal error is no longer present.

Bit 3:
CMERF – Communication (COM) Error Flag
This flag is set when a communication error is detected by the NRGC in the network between the main controller and the NRGC. This flag is cleared when no Communication error is detected by the NRGC in the in the network between the main controller and the NRGC.

Bit 4:
BSERF – Bus Communication (BUS) Error Flag
This flag is set when a communication error is detected by the NRGC in the internal BUS chain (i.e., the network between the NRGC and the RG..N end-devices). This flag is cleared when no communication error is detected by the NRGC in the internal BUS chain.

Bit 5:
DLERF – Device Limit Error Flag
This flag is set when following a Sequence Roll Call command the number of RG..Ns found on the internal bus chain is larger than the allowable maximum depending on the end device model. This flag is cleared only when the number of RG..N detected is within the allowable range after a Sequence Roll Call command is executed.

Bit 6:
DMERF – Device Mismatch Error Flag
This flag can only be set by the main controller when the result from a Roll Call or AutoConfig operation indicates that the number of RG..Ns found on the BUS chain does not match with the expected number of RG..Ns. The expected number of RG..Ns is known by the user which may program the main controller accordingly. This flag is set if the main controller issues a command to Set Device Mismatch Alarm and cleared either upon a reset of the NRGC or through a Clear Device Mismatch Alarm command.

Bit 7:
TMERF – Termination Error Flag
This flag is set when the NRGC detects that the termination of the internal BUS chain is not as expected. This check is done only at power-up of the NRGC. A reset of the NRGC is required to clear this flag. The flag is cleared only if the termination error is no longer present after a reset.

Bits 8-13:
Not used.

Bit 14:
Reserved.

Bit 15:
CTRBF – Controller Busy Flag
This flag is set whenever the NRGC is requested to perform an operation directly with the RG..Ns, for example an AutoConfig command. This flag is automatically cleared once the ongoing command is terminated. When this bit is cleared, the main controller may read the contents of the Last Operation Register (**LTOPR**), in order to know the last operation that was performed by the controller.

When this bit is set, the main controller may read the contents of the **LTOPR** in order to know the operation that is currently on-going and hence keeping the NRGC busy.

When this bit is set, the NRGC has limited access. Only the following operations are allowed:

- Reading the NRGC Status register (**CTRSR**).
- Reading the Last Operation register (**LTOPR**).
- Writing to the **CMMDB** bits in the Command and Setup Register (**CMDSTR**) to request a Communications Check Stop command when a Communications Check operation is currently ongoing. Any other request will result in an Exception Response with Exception Code 6 – meaning that the device is busy.

LTOPR – Last Operation Register

Register location - 257 (0x0101)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LTOPR [15:0]															
Status after reset	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1

Bits 0-15:
This register is used to hold the last operation that was requested to the NRGC. If the Controller Busy Flag (**CTRBF**) in the **CTRSR** is set, the Last Operation register (**LTOPR**) indicates the operation that is currently on-going. If **CTRBF** is not set, then the **LTOPR** indicates the last operation that was performed by the NRGC. The values that the **LTOPR** register can have are the following:

LTOPR Value	Operation
0x0000	No Operation
0x0001	Sequence Roll Call (requested via CMMDB)
0x0002	Presence Roll Call (requested via CMMDB)
0x0003	AutoConfig (requested via CMMDB)
0x0004	Communications Check Start (requested via CMMDB)
0x0005	Communications Check Stop (requested via CMMDB)
0x0006	Communications Settings Update (requested via CMMDB)
0x0007	Set Device Mismatch Alarm (requested via CMMDB)
0x0008	Clear Device Mismatch Alarm (requested via CMMDB)
0x0100	Communications Check Start (requested via Push Button)
0x0200	Communications Check Stop (requested via Push Button)
0xFF00	NRGC in blocked state (hex switch and/or communication parameters corrupt / illegal)
0xFF05	End-device refresh operation (following a reset event)

MBIDR – Modbus ID Register

Register location - 272 (0x0110)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									MBIDR [7:0]							
Status after reset	0	0	0	0	0	0	0	0	Refer to below							

Bits 0-7:

MBIDR – Modbus ID Register

This register holds the Modbus ID stored in the NRGC at power-up. This register is updated with this value only at power-up and shall remain unchanged until the next power-up even if this setting is changed as a result of calling a Communications Settings Update command. The expected valid ID range reported in this register should be between 1 and 247. If for some reason, the ID stored internally in the NRGC is 0, 248-255, the NRGC will automatically default to ID 1 (same as shipped value) and will also default the baud rate **MBBRR** and parity **MBPRR** to default values, i.e. 5 and 3 respectively.

Bits 8-15:

Not used.

MBBRR – Modbus BaudRate Register

Register location - 273 (0x0111)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													MBBRR [3:0]			
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	Refer to below			

Bits 0-3:

MBBRR – Modbus BaudRate Register

This register holds the Modbus BaudRate setting stored in the NRGC at power-up. It remains unchanged until the next power-up even if this setting is changed as a result of calling a Communication Settings Update command. The new setting will take effect only at the next power-up and will be reflected in this register. The expected valid values reported in this register are as follows:

Value	Mode
0x0	Not Allowed
0x1	9600
0x2	19200
0x3	38400
0x4	57600
0x5	115200 (default value)

If for some reason, the value stored internally in the NRGC is 0 or some other value than those noted in above table, the NRGC will automatically default to 115200 (same as shipped value) and will also default the ID **MBIDR** and parity **MBPRR** to default values, i.e. 1 and 3 respectively.

Bits 4-15:

Not used.

MBPRR – Modbus Parity Register

Register location - 274 (0x0112)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														MBPRR [2:0]		
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	Refer to below		

Bits 0-2:

MBPRR – Modbus Parity Register

This register holds the Modbus Parity setting stored in the NRGC at power-up. It remains unchanged until the next power-up even if this setting is changed as a result of calling a Communication Settings Update command. The new setting will take effect at the next power-up and will be then reflected in this register. The expected valid values reported in this register are as follows:

Value	Mode
0x0	Not Allowed
0x1	No parity (2-Stop Bits)
0x2	Odd (1-Stop Bit)
0x3	Even (1-Stop Bit) (default value)

If for some reason, the value stored internally in the NRGC is 0 or something else than noted in above table, the NRGC will automatically default to Even Parity (same as shipped value) and will also default the ID MBIDR and baud rate MBBDR to default values, i.e., 1 and 5 respectively.

Modbus requires that each byte transmission is made up of 11 bits. An odd or even parity setting will automatically imply 1 stop bit. If no parity is selected, the 2 stop bits will be utilised so as to keep the 11bits per character transmission.

Bits 3-15:

Not used

TPRDC – Total Present Device Counter

Register location - 258 (0x0102)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPRDC [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-15:

TPRDC – Total Present Device Counter

This counter holds the **total number of RG..Ns present** on the BUS chain connected to the NRGC. The value of this counter reads 0 after a reset of the NRGC and is updated only after a Roll Call or an AutoConfig command. Following a Roll Call or an AutoConfig command, the value of this counter will report the total number of RG..Ns detected IRRESPECTIVE of their configuration status

CCFDC – Correctly Configured Device Counter

Register location - 259 (0x0103)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCFDC [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-15:

CCFDC – Correctly Configured Device Counter

This counter holds the **total number of Correctly Configured RG..Ns present** on the BUS connected to the NRGC. The value of this counter reads 0 after a reset of the NRGC and its value is updated only after a Roll Call or an AutoConfig command. Following a Roll Call or an AutoConfig command, the value of this counter will report the total number of RG..Ns detected which were found to be CORRECTLY CONFIGURED.

For an RG..N to be considered as CORRECTLY CONFIGURED:

- The RG..N ID stored in the RG..N is within the allowed range (1 to 48 devices for RG..D..N and 1 to 32 switched poles for RG..CM..N) **AND** matches with the physical location of the RG..N on the BUS.
- The NRGC ID stored in the RG..N matches with the NRGC ID to which the RG..N is connected.

WCFDC – Wrongly Configured Device Counter

Register location - 260 (0x0104)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WCFDC [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-15:

WCFDC – Wrongly Configured Device Counter

This counter holds the **total number of Wrongly Configured RG..Ns present** on the BUS connected to the NRGC. The value of this counter reads 0 after a reset of the NRGC and its value is updated only after a Roll Call or an AutoConfig command. Following a Roll Call or an AutoConfig command, the value of this counter will report the total number of RG..Ns detected which were found to be WRONGLY CONFIGURED.

An RG..N is considered to be WRONGLY CONFIGURED if:

- The RG..N ID and the NRGC ID stored in a particular RG..N do **NOT** meet the criteria to be considered as Correctly Configured **AND** do not meet the criteria to be considered as Un-Configured.

UCFDC – Un-Configured Device Counter

Register location - 261 (0x0105)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UCFDC [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-15:

UCFDC – Un-Configured Device Counter

This counter holds the **total number of Un-Configured RG..Ns present** on the BUS connected to the NRGC. The value of this counter reads 0 after a reset of the NRGC and its value is updated only after a Roll Call or an AutoConfig command. Following a Roll Call or an AutoConfig command, the value of this counter will report the total number of RG..Ns detected which were found to be UN-CONFIGURED.

An RG..N is considered to be UN-CONFIGURED if:

- The RG..D..N ID stored in a particular RG..D..N is 255 or outside the allowed range (0, 49-254)
- The RG..CM..N ID stored in a particular RG..CM..N is 255 or outside the allowed range (0, 33-254)
- The NRGC ID stored in a particular RG..N is 255 or outside the allowed range (0, 248-254)

EDIDRaa – RG..N ID Register aa (where aa = 1 to 48)
Register location - 288 - 335 (0x0120 - 0x014F)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									EDIDB [7:0]							
Status after reset	0	0	0	0	0	0	0	0	Refer to below							

Bits 0-7:
EDIDB – End-device (RG..N) ID Bits
These bits hold the RG..N ID stored in RG..N aa, where aa = 01 to a max. of 48 depending on end device type (RG..D..N or RG..CM..N) and is the physical position of the RG..N on the BUS.
For example, RG..N 01 is a device on the bus chain physically connected to the NRGC, RG..N 02 is the next RG..N connected physically after RG..N 01, and so on.

The **EDIDB** are read from the RG..N during the Sequence/Presence Roll Call operation or written to the RG..N during an AutoConfig operation. These bits shall read 0 at reset which is a not allowed ID. The aim of these bits is purely to aid in diagnostics during configuration of the BUS to better identify any problems that can arise during the configuration process.

The RG..N ID is stored in the RG..N and not in the NRGC. It can be recalled by the NRGC only following a Sequence or Presence Roll Call or AutoConfig command.

Bits 8-15:
Not used

CNIDRaa – Controller (NRGC) ID Register aa (where aa = 1 to 48)
Register location - 352 - 399 (0x0160 - 0x018F)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CNIDB [7:0]							
Status after reset	0	0	0	0	0	0	0	0	Refer to below							

Bit 0-7:
CNIDB – NRGC ID Bits
These bits hold the NRGC ID stored in RG..N aa (where aa = 01 to 48, and is the physical position of the RG..N). Hence RG..N 01 is the first device physically connected to the NRGC, RG..N 02 is the next RG..N connected physically after RG..N 01, and so on.

The **CNIDB** are read from the RG..N during the Sequence/Presence Roll Call operation or written to the RG..N during an AutoConfig operation. These bits shall read 0 at reset which is a not allowed ID. The aim of these bits is purely to aid in diagnostics during configuration of the BUS to better identify any problems that can arise during the configuration process.

Bits 8-15:
Not used.

DCDRaa – Device (RG..N) Configuration Data Register aa (where aa = 1 to 48)
Register location - 416 - 463 (0x01A0 - 0x01CF)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								CFERF		CTCSB [2:0]				EDCSB [2:0]		
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-2:
EDCSB – End-device (RG..N) ID Configuration Status Bits
These bits hold the configuration status of RG..N ID aa (where aa = 01 to 48 and represents the physical position of the RG..N) that was determined during a Roll Call or AutoConfig operation and is based on the RG..N ID that was read from the respective RG..N.

These bits shall read 0 at reset which by default is a not present end-device. The aim of these bits is purely to aid in diagnostics during configuration of the BUS to better identify any problems that can arise during the configuration process. The possible values for these bits are as follows:

Value	Mode
0x0	Not Present Device (default value)
0x1	Un-Configured Device
0x2	Correctly Configured Device
0x3	Wrongly Configured Device

Bits 4-6:
CTCSB – NRGC ID Configuration Status Bits
These bits hold the configuration status of NRGC ID aa (where aa = 01 to 48 and represents the physical position of the RG..N) that was determined during a Roll Call or AutoConfig operation and is based on the NRGC ID that was read from the respective RG..N.

These bits shall read 0 at reset which by default is a not present end-device. The aim of these bits is purely to aid in diagnostics during configuration of the BUS to better identify any problems that can arise during the configuration process. The possible values for these bits are as follows:

Value	Mode
0x0	Not Present Device (default value)
0x1	Un-Configured Device
0x2	Correctly Configured Device
0x3	Wrongly Configured Device

Bit 8:
CFERF – Configuration Error Flag
This bit is set if an error is detected in RG..N aa during a Sequence Roll Call or AutoConfig operation. This error might be caused by a wrong communication with RG..N aa during Sequence Roll Call or AutoConfig operation.

Bits 3-7, 9-15:
Not used.

DTY1Raa – Device Type 1 Register aa (where aa = 1 to 48)
Register location - 480 - 575 (0x01E0 - 0x023F)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTYPB2 [7:0]								DTYPB1 [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

For future use.

Scope: to identify RG..N on BUS chain by function type and rating.

DTY2Raa – Device Type 1 Register aa (where aa = 1 to 48)
Register location - 480 - 575 (0x01E0 - 0x023F)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTYPB4 [7:0]								DTYPB3 [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

For future use.

Scope: to identify RG..N on BUS chain by function type and rating.

SIN1Raa – SIN-address 1 Register aa (where aa = 1 to 48)
Register location - 608 - 703 (0x0260 - 0x02BF)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SINB [15:8]								SINB [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-7: SIN Address bits
These bits hold the bits 0-7 of the 24 bit SIN address.

Bits 8-15: SIN Address bits
These bits hold the bits 8-15 of the 24 bit SIN address.

SIN2Raa – SIN-address 1 Register aa (where aa = 1 to 48)
Register location - 608 - 703 (0x0260 - 0x02BF)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NOT USED								SINB [23:16]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-7: SIN Address bits
These bits hold the bits 16-23 of the 24 bit SIN address.

Bits 8-15: not used. Will be read as 0s.

Unique SIN address of each RG..N will be marked on RG..N labelling.

5.3. RG..D..N Register Map

RG..D..N Holding Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Factory setting
Configuration	**OVLMR**	Over Voltage Limit Register	R/W	64	0047	V	1	660
	UVLMR	Under Voltage Limit Register	R/W	65	0048	V	1	0
	OCLMR	Over Current Limit Register	R/W	66	0049	A	0.01	Model dependent
	UCLMR	Under Current Limit Register	R/W	67	004A	A	0.01	0
	OFLMR	Over Frequency Limit Register	R/W	68	004F	Hz	0.01	66
	UFLMR	Under Frequency Limit Register	R/W	69	0050	Hz	0.01	44
	OTPWR	Over Temperature Pre-Warning Register	R/W	70	0051	°C	1	0
	CUHPR	Max Current Period Register	R/W	100	0064			0

RG..D..N Input Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Reading after reset
Status	**AL1SR**	Alarm 1 Status Register	R	6	0006	-	-	-
	EDGSR	End-Device General Status Register	R	7	0007	-	-	-
RG..N Parameters	**MCUR**	Max. Current Reading Register	R	8	0008	A	0.01	Measurement
	VRRDR*	Voltage RMS Reading Register	R	9	0009	V	1	Measurement
	FQRDR	Frequency Reading Register	R	10	000A	Hz	0.01	Measurement
	CRRDR	Current RMS Reading Register	R	11	000B	A	0.01	Measurement
	APRDR*	Apparent Power Reading Register	R	12	000C	VA	1	Measurement
	RPRDR*	Real Power Reading Register	R	13	000D	W	1	Measurement
	ENRDLR*	Energy Reading Low Register	R	14	000E	kWh	1	Last reading before power off
	ENRDHR*	Energy Reading High Register	R	15	000F			
	OTRDR	Running Hours - On Time Reading Register	R	16	0010	hrs	1	Last reading before power off

*Readings not available if REF terminal is not connected

5.4. RGx1A..CM..N Register Map

RGx1A..CM..N Holding Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Factory setting
Configuration	**LDOTWRR**	Load Running hours Write Register	R/W	17	0011	hrs	1	Last reading before power off
	EDCMDR	Command and Status Register	R/W	32	0020	-	-	-
	LDVREFR	Load Deviation Voltage Ref Register	R/W	60	003C	V	1	0
	LDIREFR	Load Deviation Current Ref Register	R/W	61	003D	A	0.01	0
	LDEVPR	Load Deviation Percentage Register	R/W	62	003E	%	1	10
	ALSTR	Alarm Setting Register	R/W	63	003F	-	-	-
	OVLMR	Over Voltage Limit Register	R/W	64	0040	V	1	660
	UVLMR	Under Voltage Limit Register	R/W	65	0041	V	1	0
	OCLMR	Over Current Limit Register	R/W	66	0042	A	0.01	Model dependent
	UCLMR	Under Current Limit Register	R/W	67	0043	A	0.01	0
	OFLMR	Over Frequency Limit Register	R/W	68	0044	Hz	0.01	66
	UFLMR	Under Frequency Limit Register	R/W	69	0045	Hz	0.01	44
	OTPWR	Over Temperature Pre-Warning Register	R/W	70	0046	°C	1	0
	OPSMR	Output Substitute Mode Register	R/W	110	006E	-	-	1
	OPSVR	Output Substitute Value Register	R/W	111	006F	%	1	0
	FMSTR	Firing Mode Setup Register	R/W	112	0070	-	-	1
	TMBSR	Time Base Setting Register	R/W	113	0071	s	0.1	0.1
	CTRLR	Control Level Register	R/W	130	0082	%	1	0
	ONOF0R	ON/OFF 0 Control Register	R/W	140	008C	-	-	0
	ONOF1R	ON/OFF 1 Control Register	R/W	141	008D	-	-	0

RGx1A..CM..N Input Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Reading after reset
Status	**AL1SR**	Alarm 1 Status Register	R	6	6	-	-	-
	EDGSR	End-Device General Status Register	R	7	7	-	-	-
RG..N Parameters	**MCUR**	Hold Current Reading Register	R	8	8	A	0.01	Measurement
	VRRDR*	Voltage RMS Reading Register	R	9	9	V	1	Measurement
	FQRDR	Frequency Reading Register	R	10	A	Hz	0.01	Measurement
	CRRDR	Current RMS Reading Register	R	11	B	A	0.01	Measurement
	APRDR*	Apparent Power Reading Register	R	12	C	VA	1	Measurement
	RPRDR*	Real Power Reading Register	R	13	D	W	1	Measurement
	ENRDLR*	Energy Reading Low Register	R	14	E	kWh	1	Measurement
	ENRDHR*	Energy Reading High Register	R	15	F	kWh	1	Measurement
	OTRDR	SSR Running Hours Read Register	R	16	10	hrs	1	Last reading before power off
	LDOTRDR	Load Running Hours Read Register	R	17	11	hrs	1	Last reading before power off

*Readings not available if REF terminal is not connected

5.5. RGx1P..CM..N Register Map

RGx1P..CM..N Holding Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Factory setting
Configuration	**LDOTWRR**	Load Running hours Write Register	R/W	17	0011	hrs	1	Last reading before power off
	EDCMDR	Command and Status Register	R/W	32	0020	-	-	-
	LDVREFR	Load Deviation Voltage Ref Register	R/W	60	003C	V	1	0
	LDIREFR	Load Deviation Current Ref Register	R/W	61	003D	A	0.01	0
	LDEVPR	Load Deviation Percentage Register	R/W	62	003E	%	1	10
	ALSTR	Alarm Setting Register	R/W	63	003F	-	-	-
	OVLMR	Over Voltage Limit Register	R/W	64	0040	V	1	660
	UVLMR	Under Voltage Limit Register	R/W	65	0041	V	1	0
	OCLMR	Over Current Limit Register	R/W	66	0042	A	0.01	Model dependent
	UCLMR	Under Current Limit Register	R/W	67	0043	A	0.01	0
	OFLMR	Over Frequency Limit Register	R/W	68	0044	Hz	0.01	66
	UFLMR	Under Frequency Limit Register	R/W	69	0045	Hz	0.01	44
	OTPWR	Over Temperature Pre-Warning Register	R/W	70	0046	°C	1	0
	SSRTR	Soft Start Ramping Time Register	R/W	107	006B	s	0.1	0
	SSOTR	Soft Start OFF Time Register	R/W	108	006C	s	0.1	5
	SSCLR	Soft Start Current Limit Register	R/W	109	006D	A	0.01	0
	OPSMR	Output Substitute Mode Register	R/W	110	006E	-	-	1
	OPSVR	Output Substitute Value Register	R/W	111	006F	%	1	0
	FMSTR	Firing Mode Setup Register	R/W	112	0070	-	-	5
	TMBSR	Time Base Setting Register	R/W	113	0071	s	0.1	0.1
	CVREFR	Voltage Compensation Reference Register	R/W	114	0072	V	1	0
	CTRLR	Control Level Register	R/W	130	0082	%	1	0
	ONOF0R	ON/OFF 0 Control Register	R/W	140	008C	-	-	0
	ONOF1R	ON/OFF 1 Control Register	R/W	141	008D	-	-	0

RGx1P..CM..N Input Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Reading after reset
Status	**CTRLFBR**	Control Level Feedback Register	R	5	5	%	1	-
	AL1SR	Alarm 1 Status Register	R	6	6	-	-	-
	EDGSR	End-Device General Status Register	R	7	7	-	-	-
RG..N Parameters	**MCUR**	Hold Current Reading Register	R	8	8	A	0.01	Measurement
	VRRDR*	Voltage RMS Reading Register	R	9	9	V	1	Measurement
	FQRDR	Frequency Reading Register	R	10	A	Hz	0.01	Measurement
	CRRDR	Current RMS Reading Register	R	11	B	A	0.01	Measurement
	APRDR*	Apparent Power Reading Register	R	12	C	VA	1	Measurement
	RPRDR*	Real Power Reading Register	R	13	D	W	1	Measurement
	ENRDLR*	Energy Reading Low Register	R	14	E	kWh	1	Measurement
	ENRDHR*	Energy Reading High Register	R	15	F	kWh	1	Measurement
	OTRDR	SSR Running Hours Read Register	R	16	10	hrs	1	Last reading before power off
	LDOTRDR	Load Running Hours Read Register	R	17	11	hrs	1	Last reading before power off

*Readings not available if REF terminal is not connected

5.6. RGC2/3P..N Register Map

RGC2/3P..N Holding Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Factory setting
Configuration	**LDOTWRR**	Load Running hours Write Register	R/W	31	001F	hrs	1	Last reading before power off
	EDCMDR	Command and Status Register	R/W	32	0020	-	-	-
	LDVREF12R	Load Dev Voltage Ref L1-L2 Register	R/W	60	003C	V	1	0
	LDIREF1R	Load Dev Current Ref L1 Register	R/W	61	003D	A	0.01	0
	LDVREF23R	Load Dev Voltage Ref L2-L3 Register	R/W	62	003E	V	1	0
	LDIREF2R	Load Dev Current Ref L2 Register	R/W	63	003F	A	0.01	0
	LDVREF31R	Load Dev Voltage Ref L3-L1 Register	R/W	64	0040	V	1	0
	LDIREF3R	Load Dev Current Ref L3 Register	R/W	65	0041	A	0.01	0
	LDEVPR	Load Deviation Percentage Register	R/W	66	0042	%	1	10
	ALSTR	Alarm Setting Register	R/W	70	0046	-	-	-
	OVLMR	Over Voltage Limit Register	R/W	71	0047	V	1	660
	UVLMR	Under Voltage Limit Register	R/W	72	0048	V	1	0
	OCLM1R	Over Current Limit on L1 Register	R/W	73	0049	A	0.01	Model dependant
	UCLM1R	Under Current Limit on L1 Register	R/W	74	004A	A	0.01	0
	OCLM2R	Over Current Limit on L2 Register	R/W	75	004B	A	0.01	Model dependant
	UCLM2R	Under Current Limit on L2 Register	R/W	76	004C	A	0.01	0t
	OCLM3R	Over Current Limit on L3 Register	R/W	77	004D	A	0.01	Model dependant
	UCLM3R	Under Current Limit on L3 Register	R/W	78	004E	A	0.01	0
	OFLMR	Over Frequency Limit Register	R/W	79	004F	Hz	0.01	66
	UFLMR	Under Frequency Limit Register	R/W	80	0050	Hz	0.01	44
	OTPWR	Over Temperature Pre-Warning Register	R/W	81	0051	°C	1	0
	SSRTR	Soft start Ramping Time Register	R/W	106	006A	s	0.1	0
	SSOTR	Soft start OFF Time Register	R/W	107	006B	s	0.1	5
	SSCLR	Soft Start Current Limit Register	R/W	108	006C	A	0.01	0
	LDCNCFR	Load Connection Configuration Register	R/W	109	006D	-	-	-
	OPSMR	Output Substitute Mode Register	R/W	110	006E	-	-	1
	OPSVR	Output Substitute Value Register	R/W	111	006F	-	-	0
	FMSTR	Switching Mode Setup Register	R/W	112	0070	-	-	1
	TMBSR	Time Base Setting Register	R/W	113	0071	s	0.1	0.1
	CVREFR	Voltage Compensation Reference Register	R/W	114	0072	V	1	0
	TPREFR	True Power Compensation Ref Power Register	R/W	120	0078	W	1	0
	CTRLR	Control Level Register	R/W	130	0082	%	1	0
	ONOF0R	ON/OFF 0 Control Register	R/W	140	008C	-	-	0
	ONOF1R	ON/OFF 1 Control Register	R/W	141	008D	-	-	0

RGC2/3P..N Input Registers

Category	Reference	Description	Access	Location	Location (Hex)	Unit	Resolution	Reading after reset
Status	**CTRLFBR**	Control Level Feedback Register	R	5	0005	%	1	-
	AL1SR	Alarm 1 Status Register	R	6	0006	-	-	-
	EDGSR	End-Device General Status Register	R	7	0007	-	-	-
RG..N Parameters	**VR12RDR**	Voltage RMS L1-L2 Reading Register	R	8	0008	V	1	Measurement
	VR23RDR	Voltage RMS L2-L3 Reading Register	R	9	0009	V	1	Measurement
	VR31RDR	Voltage RMS L3-L1 Reading Register	R	10	000A	V	1	Measurement
	CR1RDR	Current RMS L1 Reading Register	R	11	000B	A	0.01	Measurement
	CR2RDR	Current RMS L2 Reading Register	R	12	000C	A	0.01	Measurement
	CR3RDR	Current RMS L3 Reading Register	R	13	000D	A	0.01	Measurement
	CUH1DR	Hold Current L1 Reading Register	R	14	000E	A	0.01	Measurement
	CUH2DR	Hold Current L2 Reading Register	R	15	000F	A	0.01	Measurement
	CUH3DR	Hold Current L3 Reading Register	R	16	0010	A	0.01	Measurement
	RPRDR	Real Power Reading Register	R	17	0011	W	1	Measurement
	APRDR	Apparent Power Reading Register	R	18	0012	VA	1	Measurement
	FQRDR	Frequency Reading Register	R	19	0013	Hz	0.01	Measurement
	ENRDLR	Energy Reading Low Register	R	28	001C	kWh	1	Measurement
	ENRDHR	Energy Reading High Register	R	29	001D	kWh	1	Measurement
	OTRDR	SSR Running Hours Read Register	R	30	001E	hrs	1	Last reading before power off
	LDOTRDR	Load Running Hours Read Register	R	31	001F	hrs	1	Last reading before power off

5.7. Registers Description

5.7.1. Holding Registers

LDOTWRR – Load Running Hours Write register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDOTWRR [15:0]															
Status after reset	Last reading before power off															

Bits 0-15:
This register holds the accumulated time in hours that the output of the RG..N was switched ON. The value of this register is updated every half cycle. The initial value of this register at power-up is the last reading recording before switch OFF of the NRGC. The value of this register is in steps of 1 hour, i.e. a value of 1034 would mean 1034 hours that the output was ON during its lifetime. In case of a new SSR, this value starts from 0. The value of this register can be modified in case of a load or SSR replacement. A ‘Store Permanently’ command shall be executed after modifying the value.

EDCMDR – Command and status register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CMMDB [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0 - 7:
These bits shall hold the command that shall be executed by the RG..CM..N. Writing the value of 0 has NO effect on this register and no command will be executed. This should be avoided as this will automatically remove the traceability of the last command that was executed.

Value	Mode	Description
0	No Effect (default value)	
1	Teach Operation	The values of Vref and Iref registers will be updated by measuring the present current and voltage over a period of time. The TEACH command is refuted in case of alarms present on the system. If the TEACH is unsuccessful, the values of Vref and Iref will be cleared to 0. The status of the TEACH command can be monitored in the status register. The TEACH command does not take control of the output of the SSR, it is up to the user to issue a TEACH command when the output is switched ON with a control percentage of >20% (>25% for Phase Angle switching). The duration of the TEACH procedure shall take up to a maximum of 35s depending on the level of control percentage. A ‘Store Permanently’ command is required after a TEACH command for the values of the Vref and Iref to be saved permanently in the device for next power up. For RGx1..N, the TEACH operation is only possible if REF terminal is connected.
4	Store Permanently	The parameters set in the registers will be stored permanently and will be used upon the next NRGC power-up.
8	Clear Latched Alarms	All latched alarms will be cleared after execution of this command If the alarm recovery is set to ‘Manual’ in the Alarm setting register . In the case that the alarm recovery is set to ‘Automatic’ this command has no effect.
99	Factory reset	Resets all the device settings back to default values. The values will be reset upon the next power up of the NRGC.

LDVREFR / LDVREF12R – Load Deviation Voltage Reference (L1-L2) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDVREFR / LDVREF12R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register will hold the reference voltage (voltage reference L1-L2 for RGC2/3P..N) used for the load deviation alarm. The value of this register shall be in 1V steps, i.e. a value of 50 means 50V. The default value after a reset condition shall be 0. This register can be over-written either automatically via a TEACH command or manually by the user. The accepted values are 0 or else a value between 42V and 660V. Otherwise, the request will be rejected and the setting shall remain as in the last correct update of this register. Whenever a TEACH command is requested the value will be cleared to 0. This alarm is possible only if REF terminal is connected.

LDIREFR / LDIREF1R – Load Deviation Current Reference (L1) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDIREFR / LDIREF1R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register will hold the reference current (reference current L1 for RGC2/3P..N) used for load deviation alarm. The value of this register shall be in 0.01A steps, i.e. a value of 1150 means 11.50A. The default value after a reset condition shall be 0. This register can be over-written either automatically via a TEACH command or manually by the user. Whenever a TEACH is started, the value will be cleared to 0. The minimum allowed current can be 0, the maximum limits for each variant are listed in the table below:

Model	Current ranges	Default limit
RGC1x..25KEN	300 - 3300 (300 mA - 33 A)	3300 (33 A)
RGC1x..32KEN	500 - 3300 (500 mA - 33 A)	3300 (33 A)
RGC1x..32GEN	500 - 4700 (500 mA - 47 A)	4700 (47 A)
RGC1x..42GEN	500 - 6400 (500 mA - 64 A)	6400 (64 A)
RGC1x..62GEN	500 - 9300 (500 mA - 93 A)	9300 (93 A)
RGS1x..50KEN	300 - 5500 (300 mA - 55 A)	5500 (55 A)
RGS1x..92KEN	500 - 9900 (500 mA - 99 A)	9900 (99 A)
RGS1x..92GEN	500 - 9900 (500 mA - 99 A)	9900 (99 A)
RGC2P..25KEN	500 - 3000 (500 mA - 30 A)	3000 (30 A)
RGC2P..40GEN	1000 - 4400 (1 A - 44 A)	4400 (44 A)
RGC2P..75GEN	1000 - 8200 (1 A - 82 A)	8200 (82 A)
RGC3P..20KEN	500 - 2200 (500 mA - 22 A)	2200 (22 A)
RGC3P..30GEN	1000 - 3300 (1 A - 33 A)	3300 (33 A)
RGC3P..65GEN	1000 - 7300 (1 A - 73 A)	7300 (73 A)

LDVREF23R – Load Deviation Voltage Reference L2-L3 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDVREF23R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to LDVREFR, but holds the reference voltage value for L2-L3.

LDIREF2R – Load Deviation Current Reference L2 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDIREF2R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to LDIREFR, but holds the reference current value for L2.

LDVREF31R – Load Deviation Voltage Reference L3-L1 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDVREF31R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to LDVREFR, but holds the reference voltage value for L3-L1.

LDIREF3R – Load Deviation Current Reference L3 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDIREF3R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to LDIREFR, but holds the reference current value for L3.

LDEVPR – Load Deviation Percentage Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDEVPR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register will hold the percentage load deviation used for load deviation alarm. The value of this register shall be in 1% steps, i.e. a value of 50 means 50%. The default value after a reset condition shall be 10%. This register can be over-written to set a new Percentage load deviation. The limit values of this register are between 5 and 100%. Otherwise, the request will be rejected, and the setting shall remain as in the last correct update of this register.

ALSTR – Alarm Setting Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															ALSTB [1:0]	
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 0 – 1:
This bit defines the Alarm recovery mode.

Value	Mode	Description
0	Automatic Recovery	Alarm is cleared when the alarm condition is not present.
1	Manual Recovery	Alarm is not cleared when the alarm condition is not present. Alarm will clear only after a 'Clear Latched Alarms' command is sent.

Voltage Limit Registers

The following 2 registers, **OVLMR** and **UVLMR**, give the user the possibility to set a voltage range and get an alarm indication in case the RG..N operates outside of this range. As a default, the settings of these registers are set for a range between 0V and 660V.

OVLMR – Over-Voltage Limit Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVLMR [15:0]															
Status after reset	0	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the Over-Voltage Limit allowed for the voltage measurement. The value of this register is in 1V steps, i.e. a value of 50 means 50V and a value of 700 means 700V.
The default value after a reset condition is fixed to the factory default limit of 660V set in the RG..N. If the RG..N operates over this limit, an alarm condition is raised.
This register can be over-written. However, the new limit value cannot be larger than the fixed default value (660V) and cannot be lower than the UVLMR (Under Voltage Limit) value. In such a case, the request is rejected, and the setting remains as in the last correct update of this register.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

UVLMR – Under-Voltage Limit Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UVLMR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the Under-Voltage Limit allowed for the voltage measurement. The value of this register is in 1V steps, i.e. a value of 50 means 50V and a value of 700 means 700V.
The default value after a reset condition is fixed to the factory default limit of 0V set in the RG..N. This register can be over-written, however the value written in this register cannot be larger than the OVLMR. In such a case, the request is rejected, and the setting remains as in the last correct update of this register. An alarm is raised when the voltage measurement is below the UVLMR.
A UVLMR value >0 should only be set if the REF connection is present on the RGx1..N. If the REF connection is not present on the RG..N, the voltage measurement is 0 during SSR ON and a Voltage Out of Range alarm would be issued.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

Current Limit Registers

For RGx1..N, the following 2 registers, **OCLMR** and **UCLMR**, give the user the possibility to set a current range and get an alarm indication in case the RG..N operates outside of this range.
Similarly, for the RGC2/3P..N, the following 6 registers, **OCLM1R** and **UCLM1R / OCLM2R** and **UCLM2R / OCLM3R** and **UCLM3R**, give the user the possibility to set a current range for each phase, and get an alarm indication in case any of the phases on the RGC2/3P..N operate outside of these ranges.
As a default, the settings of these registers are set for a range between 0A and maximum rating of RG..N.

OCLMR / OCLM1R – Over Current Limit (L1) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OCLMR / OCLM1R [15:0]															
Status after reset	Model dependant															

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the Over-Current Limit allowed for the current measurement (the current measurement for phase L1 in case of RGC2/3P..N). The value of this register is in 0.01A steps, i.e. a value of 50 means 0.50A, a value of 1747 means 17.47A.

The default value after a reset condition is fixed to the default limit set in the RG..N from the factory. The default is as indicated in table below. An alarm if raised if the measured current is >OCLMR.

Model	Default limit
RGC1x..25KEN	3300 (33 A)
RGC1x..32KEN	3300 (33 A)
RGC1x..32GEN	4700 (47 A)
RGC1x..42GEN	6400 (64 A)
RGC1x..62GEN	9300 (93 A)
RGS1x..50KEN	5500 (55 A)
RGS1x..92KEN	9900 (99 A)
RGS1x..92GEN	9900 (99 A)
RGC2P..25KEN	3000 (30 A)

RGC2P..40GEN	4400 (44 A)
RGC2P..75GEN	8200 (82 A)
RGC3P..20KEN	2200 (22 A)
RGC3P..30GEN	3300 (33 A)
RGC3P..65GEN	7300 (73 A)

This register can be over-written. However, the new limit value cannot be larger than the fixed default value (RG..N maximum rating) and cannot be lower than the UCLMR (Under Current Limit) value. In such a case, the request will be rejected and the setting remains as in the last correct update of this register.
The over current limit can be switched off by setting the value to 65535.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

UCLMR / UCLM1R – Under-Current Limit (L1) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UCLMR / UCLM1R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the Under-Current Limit allowed for the current measurement (the current measurement for phase L1 in case of RGC2/3P..N). The value of this register is in 0.01A steps, i.e. a value of 50 means 0.50A, a value of 1747 means 17.47A.
The default value after a reset condition is fixed to the factory default limit of 0.00A set in the RG..N. This register can be over-written however the value written in this register cannot be larger than the OCLMR. In such a case, the request is rejected and the setting remains as in the last correct update of this register. An alarm is raised when the current measurement is below the UCLMR.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

OCLM2R – Over Current Limit L2 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OCLM2R [15:0]															
Status after reset	Model dependant															

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to OCLMR, but holds the over-current value for L2.

UCLM2R – Under-Current Limit L2 Register

Register location - 76 (0x004C)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UCLM2R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to UCLMR, but holds the under-current value for L2.

OCLM3R – Over Current Limit L3 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OCLM3R [15:0]															
Status after reset	Model dependant															

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to OCLMR, but holds the over-current value for L3.

UCLM3R – Under-Current Limit L3 Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UCLM3R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
Similar to UCLMR, but holds the under-current value for L3.

Frequency Limit Registers

The following 2 registers, OFLMR and UFLMR, give the user the possibility to set a frequency range and get an alarm indication in case the RG..N operates outside of this range. As a default, the settings of these registers are set for a range between 44Hz and 66Hz.

OFLMR – Over Frequency Limit Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OFLMR [15:0]															
Status after reset	0	0	0	1	1	0	0	1	1	1	0	0	1	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the Over-Frequency Limit allowed for the frequency measurement. The value of this register is in 0.01Hz steps, i.e. a value of 5000 means 50.00Hz, a value of 6502 means 65.02Hz.
The default value after a reset condition is fixed to the factory default limit (66.00Hz) set in the RG..N. An alarm if raised if the measured frequency is >OFLMR.
This register can be over-written. However, the new limit value cannot be larger than the fixed default value (66.00Hz) and cannot be lower than the UFLMR (Under Frequency Limit) value. In such a case, the request will be rejected and the setting remains as in the last correct update of this register.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

UFLMR – Under-Frequency Limit Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UFLMR [15:0]															
Status after reset	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the Under-Frequency Limit allowed for the frequency measurement. The value of this register is in 0.01Hz steps, i.e. a value of 5000 means 50.00Hz, a value of 6502 means 65.02Hz.
The default value after a reset condition is fixed to the factory default limit (44.00Hz) set in the RG..N. This register can be over-written however the value written in this register cannot be smaller than the fixed default value of 44.00Hz and cannot be larger than the OFLMR. In such a case, the request is rejected and the setting remains as in the last correct update of this register. An alarm is raised when the frequency measurement is below the UFLMR.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

OTPWR – Over-Temperature Pre-Warning Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTPWR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the delta temperature (i.e. the temperature below the maximum temperature limit of the RG..N) at which the RG..N will issue an over-temperature pre-warning. This is only a pre-warning and no action is taken by the RG..N. The output of the RG..N is switched OFF only when the maximum limit is exceeded.
The value of this register is in 1°C steps, i.e. a value of 25 means 25°C.
The default value after a reset condition is fixed to the factory default limit of 0 set in the RG..N. Hence, the pre-warning set point is the same as the Over-Temperature Limit meaning that no early warning is issued before the Over-Temperature Limit alarm is issued.
This register can be over-written with a new pre-warning limit. However, the new limit cannot be larger than 50°C which is the permissible delta for this register. Attempting to write values larger than 50°C will be rejected and the setting remains as in the last correct update of this register.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

CUHPR – Max. Current Period Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											CUHPB [5:0]					
Status after reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits 0-5:
This register is associated to the Max. Current Reading Register MCUR only for the RG..D..N solid state relays. The MCUR gives the maximum RMS current recorded over a number of past cycles. The number of past cycles is determined by the CUHPB in this register.
For the MCUR measurement, the highest RMS current detected in each set of 8 mains full cycles is recorded and kept in a circular buffer. Entries to this circular buffer are placed in a sequential order 1, 2, 3, etc… up to 32 and then will wrap back and start again at the location 1.

Based on the value of the CUHPB, for ex. 10, every time a new entry is made to the circular buffer (i.e., every 8 full cycles) a scan is made of the last 10 entries. So if an entry is made at location 3, a scan is made of locations 3, 2, 1, 32, 31, 30, 29, 28, 27, 26. This highest value is then reported in the CUHDR.
The default value of the CUHPR is 18 meaning that the Max. Current Register will give the maximum RMS current recorded in the past 2.88s for a 50Hz line. That is, 18 * (8*20ms) = 2.88 seconds.
18 = CUHPB; each reading is placed in the circular buffer every 8 mains full cycles (20ms for 50Hz).
The maximum allowable size for the CUHPR is 32 and the minimum is 1. Hence, it is possible through the Max. Current Register to read the maximum RMS current measured in the past 5.12 seconds for a 50Hz line.

LDCNCFR – Load Connection Configuration Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													LDCNCFR [3:0]			
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-3:
Load configuration bits. This register is associated only with the RGC2/3P..N. These bits will determine the load configuration that the End-Device shall have connected at its output. The possible combinations are the following:

Value	Description
0	Star with Neutral
1	Star without Neutral
2	Delta
3	1-P Load between L1& L2
4	1-P Load between L2 & L3
5	1-P Load between L3 & L1
6	1-P Load between L1 & N
7	1-P Load between L2 & N
8	1-P Load between L3 & N

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

SSRTR – Soft Start Ramping Time Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSRTR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the soft start ramping time if Soft Start with time is enabled. The value of this register is in 0.1 seconds, i.e. a value of 50 means 5 seconds. Soft start with time mode shall be enabled if the value of this register is greater than 0 and SSCLR is 0. If SSCLR is >0, the Soft Start with Current Limit mode is enabled.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

SSOTR – Soft Start OFF time Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSOTR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register will hold the non-firing time before soft start is reactivated. The value of this register is in steps 0.1 seconds, i.e. a value of 50 means 5 seconds. The Maximum value is 255 (25.5s). The default value on initial start up (or after reset) is 50, therefore a ramp up will occur if the output has been off for 5 seconds continuously.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

SSCLR – Soft Start Current Limit Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSCLR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the current limit value to be utilised with Soft Start with Current Limit mode. The value of this register shall be in steps of 0.01, i.e. a value of 6600 means 66A. Soft start with Current Limit mode shall be enabled if the value of this register is greater than 0. This mode will take priority over Soft Start with time mode if both the current limit (SSCLR) and the time (SSRTR) are set. The maximum value of this register is model dependent as described in the table below.

Model	Upper limit
RGC1x..25KEN	6600 (66 A)
RGC1x..32KEN	6600 (66 A)
RGC1x..32GEN	9400 (94 A)
RGC1x..42GEN	12800 (128 A)
RGC1x..62GEN	18600 (186 A)
RGS1x..50KEN	11000 (110 A)
RGS1x..92KEN	19800 (198 A)
RGS1x..92GEN	19800 (198 A)
RGC2P..25KEN	6000 (60 A)
RGC2P..40GEN	8800 (88A)
RGC2P..75GEN	16400 (164 A)
RGC3P..20KEN	4400 (44 A)
RGC3P..30GEN	6600 (66 A)
RGC3P..65GEN	14600 (146 A)

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

OPSMR – Output Substitute Mode Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														OPSMB [2:0]		
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(unless 'Store permanently' command is executed)

Bits 0-2:
These bits will determine the output state of the solid state relay after a 10 second communications timeout event. This applies only if the SSR is controlled via the bus. The possible states are:

Value	Mode	Description
0	Clear output state	The SSR will turn OFF after a communications timeout
1	Hold output state (default value)	After a communications timeout, the SSR will remain in the same output state as before the timeout
2	Set Substitute Value (requires **OPSVR**)	After a communications timeout, the device will switch to a predefined substitute control level set in the 'Output Substitute Value Register'

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

OPSVR – Output Substitute Value Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									OPSVR [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-7:
This register is used to set the value at which the control level will be after a communications timeout. This register accepts a value between 0 and 100 (i.e. 0-100%) and the default value is 0. This value is used with 'Set Substitute Value' setting in the 'Output Substitute Mode Register'. In case the firing mode is set to ON/OFF any value below 100 will indicate SSR output OFF and the value of 100 will indicate SSR output ON.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

FMSTR – Firing Mode Setup Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												FMSTR [4:0]				
Status after reset	0	0	0	0	0	0	0	0	0	0	0	Model dependant				

(unless 'Store permanently' command is executed)

Bits 0-4:
Firing Mode bits. These bits will determine the firing mode that the End-Device shall use at the output.

Value	Mode	Description
0	External Control	Control shall be applied physically via the A1, A2 terminals under the blanking cover at the bottom of the control module.*(not available for RGx1P..CM..N)*
1	ON/OFF mode	The status is obtained from the ON/OFF registers (ONOF0R, ONOF1R) Note: This is the default switching mode for RGx1A..CM..N and RGC2/3P..N.
2	Burst (requires **TMBSR**)	The timebase is set in the Timebase register (**TMBSR**) and the control level is varied in the Control level register (**CTRLR**)

3	Advanced Full cycle (AFC)	The timebase is set to 2 seconds and the control level is varied in the Control level register (**CTRLR**)
4	Distributed (C1)	The timebase is set to 2 seconds and the control level is varied in the Control level register (**CTRLR**)
5	Phase Angle	The firing angle is varied according to the value in the Control level register(**CTRLR**). Note: this is the default switching mode for RGx1P..CM..N. *(not available for RGx1A..N and RGC2P..N)*

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

TMBSR – Timebase Setting Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									OPSVR [7:0]							
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(unless 'Store permanently' command is executed)

Bits 0-7:
This register defines the time base settings for the Burst firing mode (see FMSTR register for more details). This register is in steps of 0.1s and can have a value between 0.1s and 10s. The default value shall be 1, i.e. 0.1 seconds.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

CVREFR – Voltage Compensation Reference Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CVREFR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the reference voltage user for Voltage Compensation. The value of this register is in 1V steps,i.e. a value of 50 means 50V. The max. value of this register is 660V. Voltage compensation is disabled when the value of this register is 0.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

TPREFR – True Power Compensation Reference Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPREFR [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(unless 'Store permanently' command is executed)

Bits 0-15:
This register holds the reference power user for True Power Compensation. The value of this register is in 1VW steps,i.e. a value of 50 means 50W. The max. value of this register is 65,535W. True Power compensation is disabled when the value of this register is 0.

New values (i.e. the values that overwrite the default values) are not permanently stored in the RG..N unless a 'Store Permanently' command is executed after the setting of the parameters.

CTRLR – Control Level Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										CTRLR [6:0]						
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-6:
This register defines the percentage control level of the output in the case of Burst, Advanced Full Cycle, Distributed Full Cycle and Phase Angle control methods. The allowable range of values is 0-100, which is equivalent to 0-100% control level, settable in 1% steps. The default value of this register shall be 0.

ONOF0R – ON/OFF 0 Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ONOF0R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-15:
This register will hold the SSR ON/OFF status of a bank of 16 End-Devices. Therefore, **ONOF0R** will hold the status of first 16 End-Devices on the bus, with IDs 1 to 16. Each bit in the register holds the status of an end-device on the bus. For example, **ONOF0R[0]** (bit 0) will be the SSR status of End-Device 1, **ONOF0R[1]** will be the status of End-Device 2 and so on. If the particular bit is 0, it means that the respective End-Device output is **OFF**, whereas if the bit value is 1, the End-Device output is **ON**.

The ONOFxR registers are intended to be written in broadcast mode such that with one message, all devices on one chain can be written at the same time. Therefore, the register will be written into all devices but the devices will only monitor the bit corresponding to the its ID.

This register is only used when the device firing mode is set to ON/OFF Mode. If the device is in another mode, it will still accept writing to this register but it will not be used to set device state. Nonetheless, if the mode is changed to on/off, the device will change its state according to the value which had already been written into this register.

ONOF1R – ON/OFF 1 Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ONOF1R [15:0]															
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 0-15:
Similar to ONOF0R, This register will hold the status of End-Devices 17 to 32 where **ONOF1R[0]** (bit 0) will be the SSR status of End-Device 17, **ONOF1R[1]** will be the status of End-Device 18 and so on.

This register is only used when the device firing mode is set to ON/OFF Mode, if the device is in another mode, it will still accept writing to this register but it will not be used, to set device state. Nonetheless if mode is changed to ON/OFF the device will change its state according to the value which had already been written into this register.

5.7.2. Input Registers

CTRLFBR – Control Feedback Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRLFBR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
This register contains the actual control level of the output firing. (0-100%). In the case of ON/OFF mode it shall give 0 or 100. In the case of the other firing modes it shall either reflect the value in the Control Level Register or else if voltage compensation is active than it shall contain the result of the compensation algorithm.

AL1SR – Alarm 1 Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						VCNPF	RCLMF	LDF	TOORF	OTPWF	FOORF	COORF	VOORF	EDSCF	SYF2F	SYF1F
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Refer to Section 8 for further details related to the specific alarms noted below. Each flag value is cleared when the alarm condition is no longer present on the device.

Bit 0: **SYF1F** - Mains loss Alarm Flag - this flag is set if a Mains loss is present in the RG..N.

Bit 1: **SYF2F** - Load loss / SSR open circuit Alarm Flag - this flag is set if a Load loss / SSR open circuit is present in the RG..N.

Bit 2: **EDSCF** - RG..N Short Circuit Alarm Flag - this flag is set if the RG..N is in a short-circuit condition.

Bit 3: **VOORF** - Voltage Out of Range Alarm Flag - this flag is set if the voltage measured by the RG..N is outside the default range or the set range by user. T

Bit 4: **COORF** - Current Out of Range Alarm Flag - this flag is set if the current measured by the RG..N is outside the default range or the set range by user.

Bit 5: **FOORF** - Frequency Out of Range Alarm Flag - this flag is set if the frequency measured by the RG..N is outside the default range or the set range by user.

Bit 6: **OTPWF** - Over-temperature Pre-Warning Alarm Flag - this flag is set if an over-temperature pre-warning condition is present in the RG..N.

Bit 7: **TOORF** - Temperature Out of Range Alarm Flag - this flag is set if an over-temperature condition is present in the RG..N.

Bit 8: **LDF** - Load Deviation Alarm Flag - this flag is set if a Load Deviation condition is present on the device.

Bit 9 (only for RGx1/2/3P..CM..N): **RCLMF** - Ramping Current Limit Flag - this flag is set if a Current limit condition is detected during current mode ramping.

Bit 10 (only for RGx1/2/3P..CM..N): **VCNPF** - Voltage Compensation Not Possible Flag - this flag is set if a current limit condition is detected during current mode ramping. T

11-15: Not used. These bits shall read 0.

EDGSR – End-device (RG..N) General Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				VCACTF	RAMPFL	TCHSFLF	TCHBSYF	AL1SF					CMERF	INERF	ACSWSF	DRSTF
Status after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit 0: **DRSTF** - Device Reset Flag - this is set every time the RG..N is re-setted. This bit is cleared to 0 once the **EDGSR** is read

Bit 1: **ACSWSF** - AutoConfig Switch Status Flag - this flag reflects the status of the AutoConfig line switch. If this flag is set, the RG..N has its AutoConfig switch closed. If this bit is cleared, the RG..N has its AutoConfig switch open

Bit 2: **INERF** - Internal Error Alarm Flag - this flag is set as long as an internal error is present in the RG..N. This flag is cleared once no internal error is present in the RG..N

Bit 3: **CMERF** - Communication Error Alarm Flag - this flag is set as long as a Communication error is present in the RG..N. This flag is cleared once no Communication errors are anymore present in the RG..N

Bits 4-7: not used. These bits shall read 0.

Bit 8: **AL1SF** - Alarm 1 Status Flag - this flag is set if any flag in the Alarm 1 Status Register **AL1SR** is set. This flag gives an immediate indication whether there is a condition that requires attention without the need to read the **AL1SR** periodically. The **AL1SR** is only required to be read once the **AL1SF** is read as set in order to detect the cause of the alarm condition

Bit 9: **TCHBSYF** - Teach Busy Flag - This flag is set while a TEACH operation is being executed

Bit 10: **TCHSFLF** - Teach Successful Flag - This flag is set once a TEACH operation has finished successfully. Flag is cleared once a new TEACH command is started.

Bit 11 *(only for RGx1P..CM..N)* : **RAMPFL** - Ramping Flag - This flag is set whenever ramping (soft start) is active. Flag is cleared when soft start is inactive.

Bit 12 *(only for RGx1P..CM..N)*: **VCACTF** - Voltage Compensation Active Flag - This flag is set whenever Voltage Compensation is active.

Bits 13-15: Not used. These bits shall read 0

VRRDR / VR12RDR – Voltage (L1-L2) RMS Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VRRDR / VR12RDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
This register holds the last reading of the RMS voltage (RMS voltage between L1-L2 for RGC2/3P..N). The value of this register is in 1V steps. i.e. a value of 50 means 50V and a value of 700 means 700V. If a fault occurs in the system such that it is not possible to measure the voltage, this register gives a value of 0. This value is updated every half cycle but is based on the average of the last 16 half cycles. This reading is not available if the REF terminal is not connected.

VR23RDR – Voltage L2-L3 RMS Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VR23RDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
Similar to the VR12RDR register, but holds the last reading of the RMS voltage between L2-L3 for RGC2/3P..N.

VR31RDR – Voltage L3-L1 RMS Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VR31RDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
Similar to the VR12RDR register, but holds the last reading of the RMS voltage between L3-L1 for RGC2/3P..N.

CRRDR / CR1RDR – Current RMS Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRRDR / CR1RDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
This register holds the last reading of the RMS current (RMS current through L1 for RGC2/3P..N). The value of this register is in 0.01A steps, i.e. a value of 50 means 0.50A and a value of 1747 means 17.47A. If a fault occurs in the system such that it is not possible to measure the current, this register gives a value of 0. This value is updated every half cycle but is based on the average of the last 16 half cycles.

CR2RDR – Current RMS Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CR2RDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
Similar to the CR1RDR register, but holds the last reading of the RMS current through L2 for RGC2/3P..N.

CR3RDR – Current RMS Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CR3RDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
Similar to the CR1RDR register, but holds the last reading of the RMS current through L3 for RGC2/3P..N.

CUHDR / CUH1DR – Hold Current Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CUHDR / CUH1DR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
The average current (current through L1 for RGC2/3P..N) of the last 16 ON half cycles. This measurement can be used for I^2 control. This register is available only for RG..CM..N solid state relays. The value of this register is in 0.01A steps, i.e. a value of 50 means 0.50A and a value of 1747 means 17.47A.

CUH2DR – Hold Current Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CUH2DR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
Similar to the CUH2DR register, but holds the average current through L2 for RGC2/3P..N.

CUH3DR – Hold Current Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CUH3DR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
Similar to the CUH2DR register, but holds the average current through L3 for RGC2/3P..N.

MCUR – Max. Current Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MCUR [15:0]															
Status after reset	Actual measurement															

The highest RMS value of current recorded over a past number of cycles. The number of cycles is settable in the Hold Current Period Register. This register is available only for RG..CM..N solid state relays. The value of this register is in 0.01A steps, i.e. a value of 50 means 0.50A and a value of 1747 means 17.47A

RPRDR – Real Power Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RPRDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
This register holds the real power reading in W. The value of this register is in 1W steps, i.e. a value of 567 would mean 567W. This value is updated every half cycle but is based on the average of the instantaneous voltage & current multiplications accumulated and averaged over the last 16 half cycles.

This reading is not available if REF terminal is not connected.

Note that for resistive loads with power factor = 1, the real power and the apparent power will be the same.

APRDR – Apparent Power Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	APRDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
This register holds the apparent power reading in VA. The value of this register is in 1VA steps, i.e. a value of 567 would mean 567VA. This value is updated every half cycle and is a multiplication of the Voltage RMS value and Current RMS value determined in the last half cycle.
This reading is not available if REF terminal is not connected.

FQRDR – Frequency Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FQRDR [15:0]															
Status after reset	Actual measurement															

Bits 0-15:
This register holds the last reading of the frequency. The value of this register is in 0.01Hz steps, i.e. a value of 5000 means 50.00Hz and a value of 6502 means 65.02Hz. If a fault occurs in the system such that it is not possible to measure the frequency, this register gives a value of 0. This value is updated every half cycle but is based on the average of the last 16 half cycles.

ENRDLR – Energy Reading Low Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ENRDLR [15:0]															
Status after reset	Last reading before power off															

Bits 0-15:
This register holds the lower 16 bits of the active (real) energy reading (32-bit value) in kWh. The initial value of this register at power-up is the last reading recorded before switch OFF of the NRGC. In case of a new device this value starts from 0. This register starts counting from the initial value at power-up the kWh consumed during this power up. The value of this register is in steps of 1 kWh, i.e. a value of 1034 would mean 1034kWh.
This value is updated every time the RPRDR is updated and hence every half cycle the value of the RPRDR is multiplied with the time duration of the last half cycle.

This reading is not available if REF terminal is not connected. Readings <10W are not considered.

ENRDHR – Energy Reading High Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ENRDHR [15:0]															
Status after reset	Last reading before power off															

Bits 0-15:
This register is exactly the same as the ENRDLR with the difference that it holds the upper 16 bits of the active (real) energy reading (32-bit value).

OTRDR – Running Hours (On Time) Reading Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OTRDR [15:0]															
Status after reset	Last reading before power off															

Bits 0-15:
This register holds the accumulated time in hours that the output of the RG..N was switched ON. The value of this register is updated every half cycle. The initial value of this register at power-up is the last reading recording before switch OFF of the NRGC. In case of a new device this value starts from 0. This register starts counting from the initial value at power-up the running hours during this power up. The value of this register is in steps of 1hour, i.e. a value of 1034 would mean 1034h that the output was ON during its lifetime. In the event that the counter reaches its maximum value, the counter shall roll back to 0 and start counting up again.

LDOTRDR – Load Running Hours Reading register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LDOTRDR [15:0]															
Status after reset	Last reading before power off															

Bits 0-15:
This register is a mirror of the value within LDOTWRR (Holding Register). Therefore, it will always contain the value of LDOTW.

6. Operating the NRG System

The following section describes and gives recommendations on how the NRG system can be set up and operated. The NRGC operations (when the NRGC acts as a master of the BUS chain) are explained in further details in the next sections.

6.1. Setting the NRGC Modbus ID

The main controller addresses the NRGC using its respective unique ID. Valid Modbus IDs are from 1 to 247. All other addresses are not supported and no communication will take place with NRGCs set with IDs outside the valid range. The setting of the ID for the NRGC can be done either physically through a hex switch (as explained in Section 6.1.1) or else through Modbus (as explained in Section 6.1.2).

If the hex switch is at any position other than 0, the valid NRGC ID is the ID set by the hex switch. If the hex switch is set to position 0, the valid NRGC ID is the ID stored internally in the NRGC and hence in the MBIDR.

Default shipping ID = 1 with hex switch at position 0.

6.1.1. Setting the NRGC Modbus ID through the hex switch

(Applicable only for Modbus IDs 1 to 15)

A 16-position hex switch is located behind a flap on the front face of the NRGC. The default shipping position is 0. The setting of the hex switch at position 0 means that the ID of the NRGC is taken from register MBIDR which is set to the default shipping ID of 1. Valid hex switch positions are 1-9 and A-F covering a range of IDs from 1 to 15.

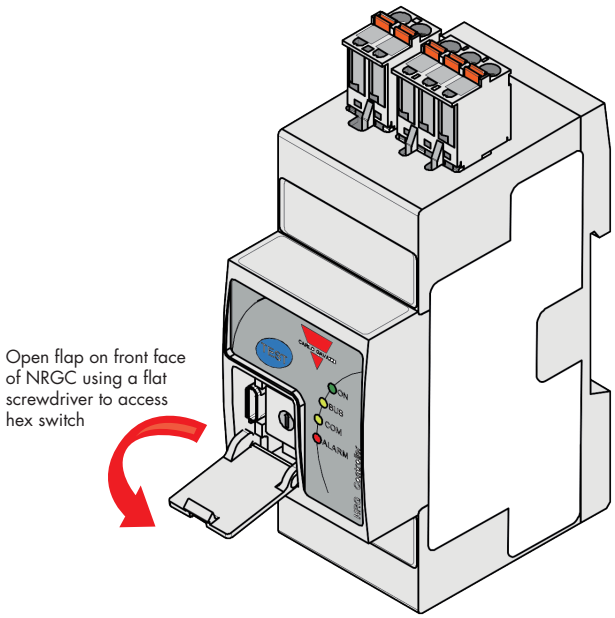


Fig. 10 - Accessing the hex switch on the NRGC

The hex switch shall be positioned to the desired ID, 1-9 or A-F (for IDs 10-15). It is not required that the NRGC is powered during this setting procedure. The set ID shall come in effect at the next power up of the NRGC.

Changing the hex switch position during operation (i.e., with the NRGC powered and in operation) shall have no effect. It is necessary to reset the NRGC supply voltage for the new set ID to become effective.

Make sure that when configuring the NRGC ID there are no other devices in the same Modbus chain with the same ID. In such a case, it will be impossible for the main controller to communicate with the devices present on the BUS and abnormal behaviour of the whole serial BUS may occur.

6.1.2. Setting the NRGC Modbus ID through Modbus using the STIDR

(Applicable for Modbus IDs 1 to 247)

In this case, the hex switch referred to in Section 6.1.1 has to be set to position 0 (which is the default shipping position). Position 0 of the hex switch makes reference to the NRGC ID stored internally in the MBIDR which is set to 1 as the default shipping ID.

For this procedure, the NRGC must be powered up to enable communication. Since the NRGC needs to be accessed through an RS485 link, the respective ID and communication settings of the NRGC to be addressed need to be known beforehand. Default shipping BaudRate is 115200 bits/s and default shipping parity is even.

The required ID, which can be 1 to 247, is written to the STIDR of the respective NRGC. This shall be followed by a request for a Communications Settings Update (refer to Section 6.2 for further details). The new NRGC (internal) ID shall take effect at the next power up of the NRGC and as long as the hex switch is set to position 0.



It is suggested that each NRGC is accessed individually for the setting of the ID to avoid collisions with other devices on the BUS.



In case the internal NRGC ID has been changed from its shipped default of 1 and the currently set ID is not known it is suggested to proceed as follows:

- set the NRGC to a new ID by making use of the hex switch (for example, position 5 for NRGC ID 5)
- make this new NRGC ID effective by powering OFF and ON again the NRGC
- use the new ID, 5, and known communication settings to write the desired ID to the STIDR and request a Communications Settings Update
- set hex switch to position 0
- reset the NRGC

6.2. Procedure for executing a Communication Settings Update operation

The NRGC is shipped with default settings for ID, BaudRate and parity. The ID of the NRGC can be set as indicated in Section 6.1. In case an NRGC ID in the range 16 to 247 is required the hex switch cannot be used and the required ID is updated through the STIDR. In this case the hex switch has to be set to position 0.

The default BaudRate and parity settings can be updated from the STBRR and STPRR respectively.

The new communication settings are effective only after a Communication Settings Update command (executed as explained in the following), followed by a reset of the NRGC.

Steps	Remarks
1. Update registers **STIDR, STBRR**, **STPRR** with the required values.	This shall be done before requesting a Communications Settings Update operation.
2. The main controller should first read the **CTRSR.**	This is to ensure that the **CTRBF** is clear and hence there is no on-going operation in the NRGC and that there are no internal errors present in the NRGC.
3. In case of an ongoing operation in the NRGC, the **CTRBF** shall be polled until found clear.	No commands are accepted unless this flag is clear.
4. In case of an error in the NRGC, this shall first be cleared.	Refer to Section 9 for Troubleshooting aids.
5. The main controller shall request a Communication Settings Update command using code **0x06** in the **CMMDB** of the **CMDSTR.**	
6. A positive reply is sent back to the main controller if the operation request was accepted by the NRGC.	The **CTRBF** is not set with a Communication Settings Update operation. Hence, another command can be immediately requested to the NRGC after a reply that the command was accepted is received.
7. Reset the NRGC for the updated communication settings to become effective.	The Communication Settings Update operation updates the values of all the following registers **STIDR, STBRR** and **STPRR.** On power-up, the NRGC sets the initial values of the **STIDR**, **STBRR** and **STPRR** to the internal settings currently stored in the NRGC. This is done so that just in case only one register needs to be updated the registers that are not updated would have the current set values.

6.3. Procedure at power-up

A reset of the NRGC, occurring from a machine start-up or a reset of the NRGC supply voltage, can be identified by the NRGC Reset Flag **CRSTF** which will be set in the NRGC Status Register **CTRSR**.

The following is a recommended procedure that the main controller should perform at every power up of the NRGC (that is every time the **CRSTF** is set) since some registers (e.g. counters, limit registers, etc.) are not permanently stored and data is lost upon a reset of the NRGC. This procedure has to be repeated for every NRGC present in the system:

Steps	Remarks
1. On power up of the system, the main controller should first read the **CTRSR** of the respective NRGC.	The **CRSTF** in the **CTRSR** is set at every power up of the NRGC to indicate such an occurrence. Read-out of the **CRSTF** clears this flag.
2. The main controller should confirm that no alarms reside in the NRGC. In case of errors in the NRGC these should be tackled before proceeding further.	Refer to Section 9 for Troubleshooting aids. As long as communication between the main controller and the NRGC and RG..Ns is possible, information from RG..Ns may still be retrieved.
3. It is possible for the main controller to proceed in either of the following ways: • Start communication with RG..Ns • Request a Sequence Roll Call operation • Request an AutoConfig operation	Communication with RG..Ns: This is only possible if the RG..Ns have been previously configured and have a valid ID. Brand new units are shipped in an un-configured state and communication with new RG..Ns is not possible before an AutoConfig operation. Starting communication with RG..Ns without first performing a Sequence Roll Call operation is done at the risk that some RG..Ns might be faulty and/or are not correctly configured and/or are not in the correct physical position. This would result in RG..Ns that might not reply or may result in a collision of RG..Ns that might have the same IDs. Request a Sequence Roll Call operation: This is the recommended option to ensure that all RG..Ns connected on each BUS chain are correctly configured and communicating correctly. Refer to Section 6.6 for further details. Request an AutoConfig operation: This should ideally be preceded by a Sequence Roll Call to ensure correct system status before permanently assigning an ID to the RG..Ns on the BUS chain. This operation is necessary for brand new units which are shipped in an unconfigured state that need to be correctly configured to enable communication with the NRGC and the main controller.
4. Once the main controller establishes communication directly with the RG..Ns, it should: • Update default limit settings of the RG..Ns (if required) • Read the required parameters from the RG..Ns	Refer to Section 4.8.3 for further details on communication with RG..Ns.

6.4. Procedure during operation

Steps	Remarks
1. The main controller should read the NRGC Status Register, **CTRSR** periodically to ensure that no abnormal condition occurred in the NRGC.	By reading the **CTRSR** it is possible to identify: • that no accidental reset of the NRGC occurred. If the **CRSTF** is set, this means that the NRGC has undergone a reset event. • that no internal errors are present in the NRGC, i.e. the **INERF** is clear. • that no communication errors are reported by the NRGC in the link between the NRGC and the main controller, i.e. the **CMERF** is clear. • that no communication (BUS) errors are reported by the NRGC in the link between the NRGC and RG..Ns, i.e. the **BSERF** is clear. • that a device mismatch error and/or a device limit error are not present in the NRGC, i.e. the **DMERF** and **DLERF** are clear. • that a termination error was not detected at power-up, i.e. **TMERF** is clear.
2. The main controller should read the respective RG..N Status Register (**EDGSR**) periodically to ensure that no abnormal condition occurred in the respective RG..N.	By reading the **EDGSR** it is possible to identify: • that no accidental reset of the RG..N occurred. If the **DRSTF** is set, this means that the RG..N has undergone a reset event. • that no internal errors are present in the RG..N, i.e. the **INERF** is clear. • that no communication (BUS) errors are reported by the RG..N in the link between the RG..N and the NRGC, i.e. the **CMERF** is clear. • that no alarm is present on the RG..N, i.e. the **AL1SF** is clear.

6.5. Procedure for executing a Sequence Roll Call / Presence Roll Call / AutoConfig operation

Steps	Remarks
1. The main controller should first read the **CTRSR** of the respective NRGC.	This is to ensure that the **CTRBF** is clear and that there is no on-going operation in the NRGC and that there are no internal errors present in the NRGC.
2. In case of an ongoing operation in the NRGC, the **CTRBF** shall be polled until found clear.	No commands are accepted unless this flag is clear..
3. In case of an error in the NRGC, this shall first be cleared.	Refer to Section 9 for Troubleshooting aids.
4. The main controller shall request a command by writing the respective command code (depending on the required operation) in the **CMMDB** of the **CMDSTR.**	Command code: • 0x01 for a Sequence Roll Call operation • 0x02 for a Presence Roll Call operation • 0x03 for an AutoConfig operation
5. An exception response using Exception code 5 is sent back to the main controller if the command is accepted.	Exception code 5 indicates that the request was acknowledged and that the NRGC shall become busy to carry out the requested operation.
6. The **CTRBF** is set (busy) whilst the requested operation is ongoing and cleared once the operation is completed.	The main controller shall poll the **CTRBF** once the requested command is accepted. All NRGC registers (both input and holding) are blocked for access when the **CTRBF** is set. The only exception is read only access of the **CTRSR** and the **LTOPR**. Any request to read/write any other NRGC register shall result in a rejection of the request (exception response with exception code 6 - meaning device is busy). While the NRGC is busy, any request by the main controller directed to the RG..Ns is ignored and no reply shall be sent back to the main controller.
7. The operation procedure terminates when the main controller reads the **CTRBF** as cleared	**CTRBF** clear means there is no ongoing operation.

6.6. Procedure to check the result of a Sequence Roll Call operation

Before starting communication with the RG..Ns it is recommended to first perform a Sequence Roll Call operation to ensure that all the RG..Ns connected to a particular NRGC are correctly configured and communicating correctly. This operation will update the counters TPRDC (Total Present Device Counter), CCFDC (Correctly Configured Device Counter), WCFDC (Wrongly Configured Device Counter), and UCFDC (Un-Configured Device Counter).

If everything is in order, the result of the **TPRDC**, **CCFDC**, **UCFDC** and **WCFDC** after a Sequence Roll Call is:

- **CCFDC** = **TPRDC** = Expected no. of end-devices (RG..Ns)
- **WCFDC** = 0
- **UCFDC** = 0

In this case the main controller can start communicating with the RG..Ns

If after a Sequence Roll Call, **TPRDC**, **CCFDC**, **WCFDC**, **UCFDC** do not match the result above, the following options are possible:

- Perform a Presence Roll Call operation
- Perform an AutoConfig operation
- Proceed with system operations despite the non-ideal result from the Sequence Roll Call

Refer to Section 9.1 which covers the different scenarios that could give a result other than ideal, and how these scenarios could be managed.

6.7. Procedure to check the result of a Presence Roll Call operation

A Presence Roll Call operation may be carried out if the result from a Sequence Roll Call operation indicates that something is not in order.

During a Presence Roll Call the NRGC communicates only with the RG..Ns that are correctly configured. This operation will update the counters **TPRDC, CCFDC, WCFDC** and **UCFDC**. After a Presence Roll Call, **WCFDC** and **UCFDC** should read 0 and the **TPRDC** should be equal to **CCFDC**.

- The **TPRDC** may be equal to the expected no. of RG..Ns
  - in this case, the Presence Roll Call gives a confirmation that all RG..Ns expected to be on the BUS are actually on the BUS though maybe not in the correct physical location.

Since the Presence Roll Call does not use the auto-configuration mechanism used in the Sequence Roll Call, it is possible that after a Presence Roll Call, undetected RG..Ns in the Sequence Roll Call are identified to be present on the BUS. This might happen if an RG..N has an issue with the AutoConfiguration mechanism and cannot be detected during the scanning by the Sequence Roll Call operation.

- The **TPRDC** may NOT be equal to the expected no. of RG..Ns
  - in this case, less RG..Ns than expected were found present on the BUS

This might happen if an RG..N has an issue other than with the auto-configuration mechanism, such as an issue with communications or if an RG..N was removed from the BUS and not re-installed.

In this case the main controller has to decide whether to proceed with systems operations as explained in further detail in Section 9.1 Case 4.

6.8. Procedure to check the result of an AutoConfiguration operation

The AutoConfig operation may be requested if the result from a Sequence Roll Call operation is not as expected (refer to Section 9.1 for further details).

After an AutoConfig operation the contents of **CCFDC, TPRDC, UCFDC** and **WCFDC** are updated and should be as follows:

- **CCFDC** = **TPRDC** = Expected no. of end-devices (RG..Ns)
- **WCFDC** = 0
- **UCFDC** = 0

The main controller can communicate with each RG..N

If the contents of **CCFDC, TPRDC, UCFDC** and **WCFDC** are other than as indicated above, refer to Section 9.2 on further possible actions.

6.9. Procedure for setting / clearing a Device Mismatch Alarm

This is an optional feature that can be used to facilitate troubleshooting. The number of RG..Ns connected on each BUS chain is a decision of the machine builder. This number should not exceed the maximum allowable range for the RG..N type but can be less. The machine builder can use the Device Mismatch Alarm to facilitate diagnostics in case more or less RG..Ns than expected are connected on the BUS chain.

This mismatch could result from a mistake in panel assembly or removal of RG..Ns from the BUS chain during machine lifetime. When the number of RG..Ns detected on the BUS chain is not as expected, the Set Device Mismatch Alarm can be requested by the machine controller to the respective NRGC that will highlight this error on its respective Alarm LED and also sets the **DMERF**. The setting of the **DMERF** can be used to alert this failure to the machine user on the machine HMI indicating possible corrective actions.

The Device Mismatch Alarm can be cleared by the machine controller that requests a Clear Device Mismatch Alarm operation or by resetting the NRGC.

Set Device Mismatch Alarm:

Steps	Remarks
1. The main controller should first read the **CTRSR** of the respective NRGC.	This is to ensure that the **CTRBF** is clear and that there is no on-going operation in the NRGC and there are no internal errors present in the NRGC.
2. In case of an ongoing operation in the NRGC, the **CTRBF** shall be polled until found clear.	No commands are accepted unless this flag is clear.
3. In case of an error in the NRGC, this shall first be cleared.	Refer to Section 9 for troubleshooting help..
4. The main controller shall request a Set Device Mismatch Alarm operation using code **0x07** in the **CMMDB** of the **CMDSTR.**	
5. A positive reply is sent back to the main controller if the operation request was accepted by the NRGC.	The **CTRBF** is not set with a Set Device Mismatch Alarm operation. Therefore, another command can be immediately requested to the NRGC after a reply that the command was accepted is received.
6. The **DMERF** in the **CTRSR** is set.	A set **DMERF** triggers the Configuration Error on the Alarm LED of the NRGC (2 flashes) and the auxiliary EMR, unless this is configured otherwise.

Clear Device Mismatch Alarm:

Steps	Remarks
1. The main controller should first read the **CTRSR** of the respective NRGC.	This is to ensure that the **CTRBF** is clear and that there is no on-going operation in the NRGC and there are no internal errors present in the NRGC.
2. In case of an ongoing operation in the NRGC, the **CTRBF** shall be polled until found clear.	No commands are accepted unless this flag is clear.
3. In case of an error in the NRGC, this shall first be cleared	Refer to Chapter 7 for Troubleshooting aids
4. The main controller shall request a Clear Device Mismatch Alarm operation using code **0x08** in the **CMMDB** of the **CMDSTR.**	
5. A positive reply is sent back to the main controller if the operation request was accepted by the NRGC.	The **CTRBF** is not set with a Clear Device Mismatch Alarm operation. Therefore, another command can be immediately requested to the NRGC after a reply that the command was accepted is received.
6. The **DMERF** is cleared in the **CTRSR.**	A clear **DMERF** clears the Configuration Error on the Alarm LED of the NRGC and the auxiliary EMR if set accordingly.

6.10. Procedure for executing a Communications Start / Stop operation

The main aim of this operation is to facilitate fault finding. It provides a means to enable checking of the BUS and hence the communication link between the NRGC and the RG..Ns.

Once a Communications Check Start command is issued, the communications check operation lasts indefinitely until stopped by a Communications Check Stop command. During the communications check the NRGC attempts to communicate with each RG..N present on the BUS. In case of successful communication, the BUS LED of the respective RG..N will flash to give a visual indication of on-going communication. This operation continues until a Communications Check Stop command is issued or until a powering OFF of the system.

This operation gives also a visual indication of the RG..Ns that are detected by the NRGC. If for example, 51x RG..Ns are connected to 1x NRGC, the last 3 RG..Ns will not show any sign of communication (BUS LED OFF). This is because these RG..Ns are not recognised by the NRGC since the maximum number of RG.. Ns that the NRGC recognises is limited to 48.

Communications Check Start:

Steps	Remarks
1. The main controller should first read the **CTRSR** of the respective NRGC.	This is to ensure that the **CTRBF** is clear and that there is no on-going operation in the NRGC and there are no internal errors present in the NRGC.
2. In case of an ongoing operation in the NRGC, the **CTRBF** shall be polled until found clear.	No commands are accepted unless this flag is clear.
3. In case of an error in the NRGC, this shall first be cleared.	Refer to Section 9 for troubleshooting help.
4. The main controller shall request a Communications Check Start operation using code **0x04** in the **CMMDB** of the **CMDSTR.**	
5. An exception response using Exception code 5 is sent back to the main controller if the command is accepted.	Exception code 5 indicates that the request was acknowledged and that the NRGC shall become busy to carry out the requested operation.

6. The **CTRBF** is set (busy) whilst the requested operation is ongoing. This is cleared only when a Communications Check Stop operation is executed	The main controller shall poll the **CTRBF** once the requested command is accepted. All NRGC registers (both input and holding) are blocked for access when the **CTRBF** is set. The only exceptions are: • Read-only access of the **CTRSR** and the **LTOPR** • Write access to the **CMMDB** in order to be able to issue a **Communication Check Stop** request. Any other write request to the **CMMDB** is rejected Any request to read/write any other NRGC register shall result in a rejection of the request (exception response with exception code 6 - device is busy). While the NRGC is busy, any request by the main controller directed to the RG..Ns is ignored and no reply shall be sent back to the main controller.

Communications Check Stop:

Steps	Remarks
1. The main controller should first read the **CTRSR** of the respective NRGC.	The **CTRBF** must be found set due to a previous Communications Check Start operation initiated via the **CMMDB**. A confirmation of this can be done by reading the contents of the **LTOPR** which contents should read 0x04, i.e. Communications Check Start
2. If the **CTRBF** is set due to a Communication Check Start operation, the main controller can request a Communications Check Stop command by writing code **0x05** in the **CMMDB** of the **CMDSTR.**	
3. An exception response using Exception code 5 is sent back to the main controller if the Communications Check Stop command is accepted	Exception code 5 indicates that the request was acknowledged and that the NRGC shall become busy until the communications Check operation is actually stopped. The main controller should poll the **CTRBF** to ensure it is clear before issuing a new command.

7. Functions

7.1. Functions Overview

The NRG solid state relays are equipped with a range of functionality within one device. For a list of some of the features refer to the table below.

Feature	RG..D..N	RGx1A..CM..N	RGx1P..CM.. N	RGC2/3P..N
External Control	●	●	-	●
Control over BUS	-	●	●	●
ON/OFF mode	●	●	●	●
Burst Firing mode	●	●	●	●
Distributed full cycle Firing mode	●	●	●	●
Advanced full cycle Firing mode	●	●	●	●
Phase angle Firing mode	-	-	●	●
Soft start with time mode	-	-	●	●
Soft start with current limit mode	-	-	●	●
Voltage compensation	-	-	●	●
True power compensation	-	-	-	●
Monitoring of system parameters	●	●	●	●
SSR diagnostics	●	●	●	●
Load diagnostics	●	●	●	●
Over-temperature protection	●	●	●	●

7.2. Switching Modes

ON/OFF mode

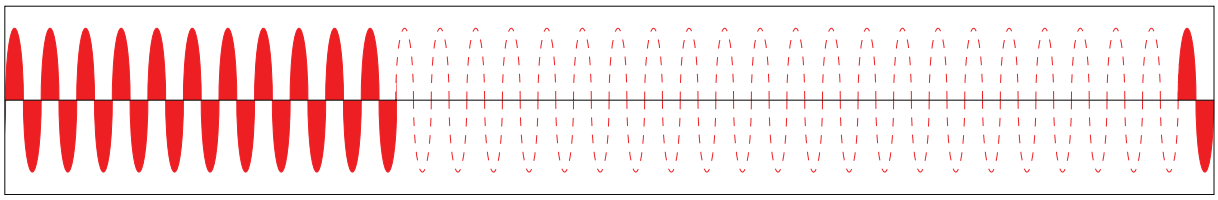
The ON/OFF mode controls the solid state relays at the user's command. Through an I/O output message, the RG..N can be controlled using the control level. A control level of 0% indicates SSR output OFF and a control level of 100% indicates SSR output ON.
The advantages of this mode are:

- It is effectively a direct replacement of the A1-A2 signal and the control algorithm within the PLC can be left relatively untouched, with the output being controlled via the communication interface.
- All RG..Ns on the bus chain can be controlled within 10ms.

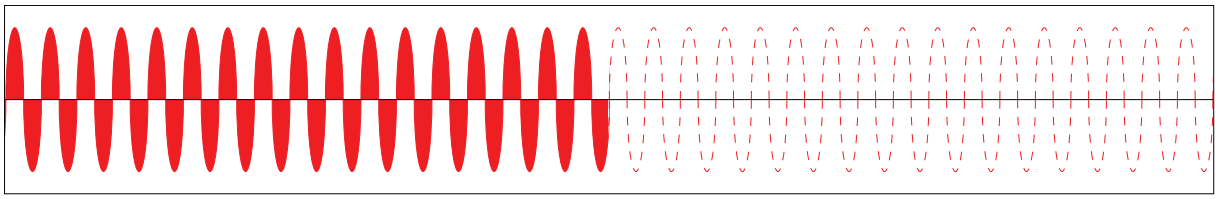
Burst Firing mode

The Burst firing mode works with the control level and a time-base parameter which can be varied from 0.1 seconds to 10 seconds. The percentage ON time is then determined by the control level via an I/O output command. Therefore, with a control level of 10% ;10% of the time-base will be ON and 90% will be OFF. The figures below show example waveforms of this firing mode at different control levels. In this example, the time base was set to 1 second. The percentage control resolution depends on the time base set by the user. To achieve a 1% resolution, the time base has to be a minimum of 2 sec for 50Hz and 1.7 sec for 60Hz.

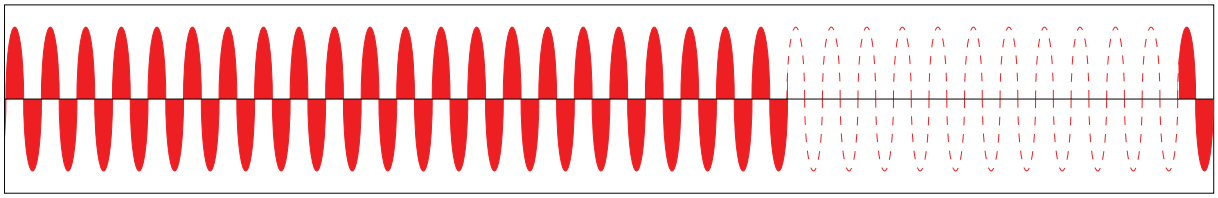
Output with Burst firing mode @ 33% control level



Output with Burst firing mode @ 50% control level



Output with Burst firing mode @ 66% control level

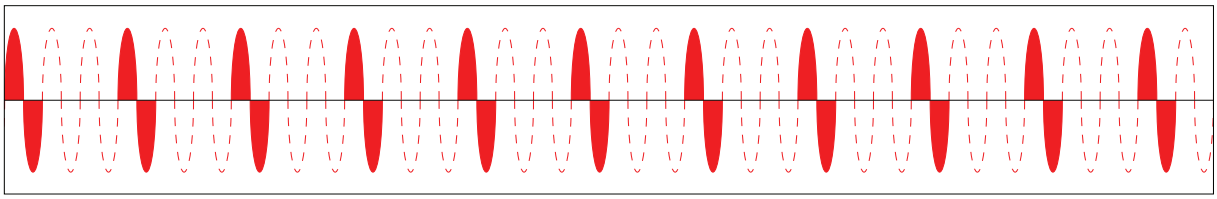


Distributed full cycle Firing mode (1x full cycle switching)

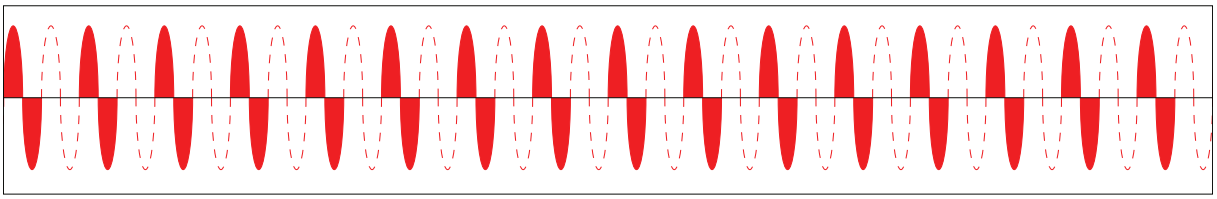
The Distributed firing mode works with a control level and a fixed time-base of 100 full cycles (2 seconds for 50 Hz). This mode operates with full cycles and it distributes the ON cycles as evenly as possible over the time base. In this mode, since the resolution is 1% and the time base is of 100 full cycles, the control level is equal to the number of full cycles over the whole time base.

1% = 1 full cycle every 100 cycles
2% = 2 full cycles every 100 cycles = 1 full cycle every 50 cycles

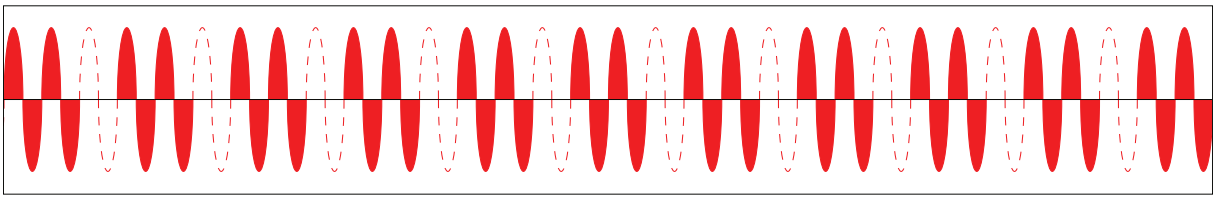
Output with Distributed firing mode @ 33% control level



Output with Distributed firing mode @ 50% control level



Output with Distributed firing mode @ 66% control level

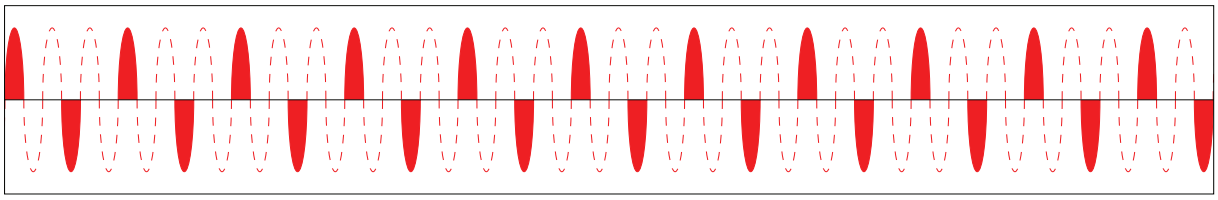


The advantage of Distributed firing over Burst firing is the reduction in thermal cycling. On the other hand, the Distributed firing mode suffers from worse harmonics/emissions than the Burst firing mode.

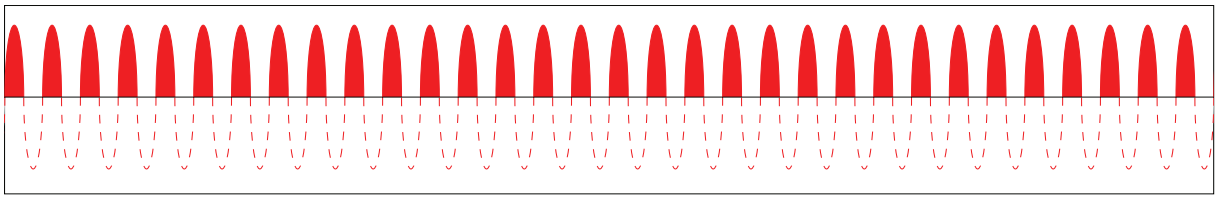
Advanced full cycle Firing mode

Advanced Full Cycle (AFC) firing works on the same concept as Distributed firing, but rather than distributing full cycles, it distributes half cycles. This mode also works over a time base of 100 full cycles (200 half cycles). In this mode, since the resolution is 1% and the time base is of 100 full cycles, the control level is equal to the number of full cycles over the whole time base. 1% = 2 half cycles every 200 half cycles = 1 half cycle every 100 half cycles, 2% = 4 half cycles every 200 half cycles = 1 half cycle every 50 half cycles.

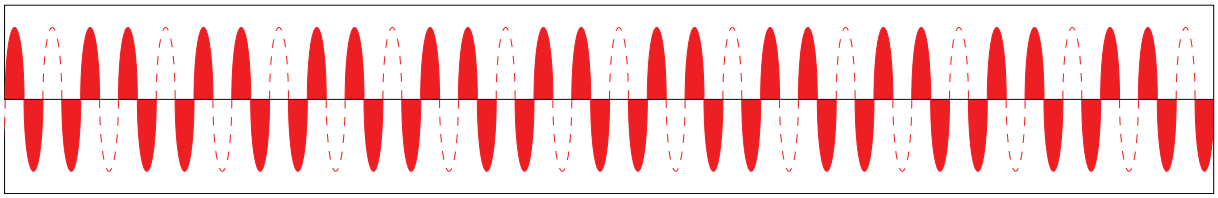
Output with Advanced full cycle firing mode @ 33% control level



Output with Advanced full cycle firing mode @ 50% control level



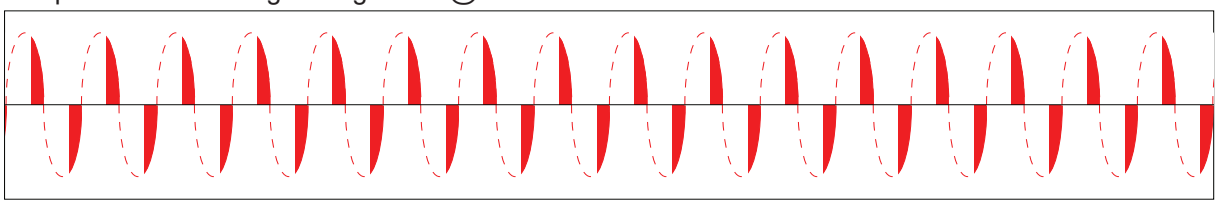
Output with Advanced full cycle firing mode @ 66% control level



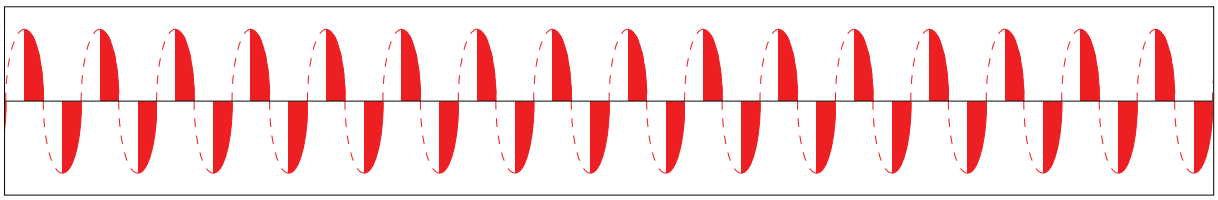
Phase Angle Firing mode

The Phase angle switching mode is available on the RGx1/3P..N solid state relays and works in accordance with the phase angle control principle. The power delivered to the load is controlled by the firing of the thyristors over each half mains cycle. The firing angle depends on the control level that determines the output power to be delivered to the load. The power to the load is varied linearly with the control level.

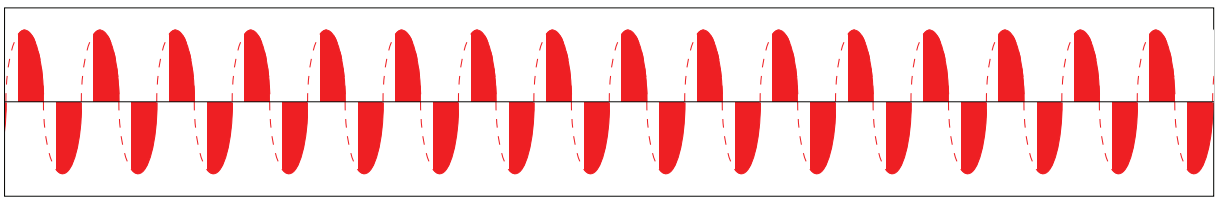
Output with Phase angle firing mode @ 33% control level



Output with Phase angle firing mode @ 50% control level



Output with Phase angle firing mode @ 66% control level

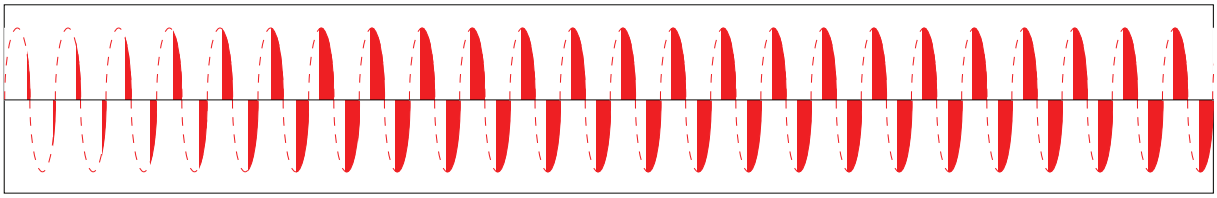


The advantage of Phase angle over the other switching modes is its precise resolution of power. However, Phase angle generates excessive harmonics vs other switching modes. With Phase angle control, the flickering of IR heaters is eliminated completely.

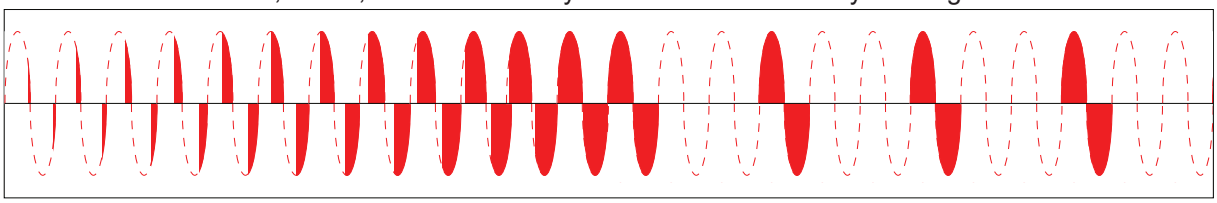
Soft Starting

Soft starting is utilised to reduce the start-up current of loads having a high cold-to-hot resistance ratio such as short wave infrared heaters. The thyristor firing angle is gradually increased in order to apply the power to the load smoothly. Soft start can be applied with all the other available switching modes: ON/OFF, Burst, Distributed full cycle, Advanced full cycle and Phase angle. When applied with phase angle, the soft start will stop at the set control level whereas for the other switching mode the soft start will stop when fully ON. Soft start shall be applied upon power up (i.e. on first application of the control signal) and after a number of non-firing cycles settable by the user (i.e. re-applying the control signal after the output is switched OFF for a period of time > OFF time to soft start setting).

Soft start with Phase angle



Soft start with ON/OFF, Burst , Distributed full cycle and Advanced full cycle firing modes



There are two type of soft start modes:

Soft start with time mode
The soft start will apply the power smoothly to the load over a time period of maximum 25.5s. This is settable via the communication system (Soft start ramping time setting).

Soft start with current limit mode
This soft start mode works with a current limit set by the user via the communication. The soft start time will adapt such that the set current limit is not exceeded, and the soft start occurs in the shortest amount of time. The recommended setting for the current limit is 1.2 - 1.5 times the nominal current. The maximum settable current limit is 2 times the rated current of the RG..CM..N variant used. If the current limit is set too low and the current limit is reached, a warning message will be triggered (Soft start current limit reached).

Voltage compensation

When voltage compensation is utilised, the output power on the output of the solid state relay will remain balanced despite any voltage deviations from normal readings. The algorithm uses a reference voltage set by the user via the communication (Voltage compensation setting) to compute the compensation factor. A new control level is calculated by applying the compensation factor on the control level from the main controller.

The compensation factor (C.F.) applied on the control level is calculated as follows:

$$\text{C.F.} = \left(\frac{\text{Reference Voltage}}{\text{Measured Voltage}} \right)^2$$

If the calculated control level after the compensation factor is applied is beyond the control level limits (0 & 100%), the absolute limit will be applied (0 or 100%) and a warning message will be triggered (Voltage compensation not possible).

External Firing mode

The RG..N can also be controlled externally via the A1,A2 terminal behind the blanking cover. For further information on the technical specifications of the input terminal, please refer to the product datasheet. External firing is only available on the RGx1A..CM..N and RGC2/3P..N solid state relays.

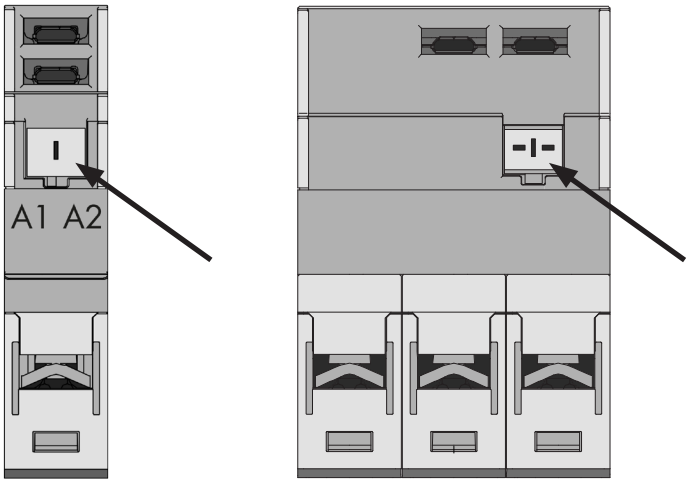


Fig. 11 - Blanking cover at the bottom of RG..N to be removed for external control (RGM25 plug is required - not included in packaging)

Note: For percentage power control switching modes (Burst, Distributed Full cycle, Advanced Full cycle and Phase Angle), the response time for each RG..N on the bus chain shall increment by a half mains cycle with each device. Therefore:
- with 32 x RGx1..N devices on the bus chain (max); all RG..Ns are controlled within 267ms (60Hz) or 320ms (50Hz) depending on the cycle time.
- with 16 x RGC2P..N devices on the bus chain (max); all RG..Ns are controlled within 133ms (60Hz) or 160ms (50Hz) depending on the cycle time.
- with 10 x RGC3P..N devices on the bus chain (max); all RG..Ns are controlled within 83ms (60Hz) or 100ms (50Hz) depending on the cycle time.
- with any combination of N x RGx1/2/3..N devices on the bus chain, all RG..Ns are controlled within N x 8.3ms (60Hz) or N x 10ms (50Hz).

7.3. Measurements

Voltage RMS / Voltage L1-L2 RMS / Voltage L2-L3 RMS / Voltage L3-L1 RMS

The last reading of the RMS voltage is recorded. The value of the reading is in 1V steps hence a value of 50 means 50V, a value of 600 means 600V. If a fault occurs in the system such that it is not possible to measure the voltage, the reading is 0. The reading is updated every half cycle based on the average of the last 16 half cycles.
For RGx1..N, this reading requires the 'Ref' terminal to be connected. If the Ref terminal is not connected this register reads the on-state voltage of the RG..N when the output is ON.
For RGC2/3P..N, three line-to-line voltages are measured (L1-L2, L2-L3, L3-L1) and no Ref connections are required.

Current RMS / Current L1 RMS/ Current L2 RMS / Current L3 RMS

The last reading of the RMS current is recorded. This reading is in steps of 0.01A hence a value of 50 means 0.5A and a value of 1747 means 17.47A. If a fault occurs in the system such that it is not possible to measure the current, this value is 0. This reading is updated every half cycle but is based on the average of the last 16 half cycles.
For RGC2/3P..N, three RMS current measurements are available (L1, L2, L3). The values are either line or phase currents depending on the load configurations

Frequency RMS

The last reading of the frequency is recorded. The value is in steps of 1 Hz. If a fault occurs in the system such that it is not possible to measure the frequency, this register gives a value of 0. This value Is updated every half cycle but is based on the averaged value of the last 15 cycles.

Hold Current / Hold Current L1 / Hold Current L2 / Hold Current L3

The average current of the last 16 ON half cycles. This value is in steps of 0.01A hence a value of 50 means 0.5A and a value of 1747 means 17.47A.
For the RGC2/3P..N, three hold current measurements are available for each phase (L1, L2, L3) for all switching modes except Advanced Full Cycle.

This measurement can be used as feedback current for an I^2 control feedback loop.

Apparent Power

The apparent power reading is recorded in VA. This reading is in steps of 1VA for RGC1..N and 10VA for RGC2/3P..N. This value is updated every half cycle and is a multiplication of the Voltage RMS value and Current RMS value determined in the last half cycle.
For RGC1..N, this reading requires the 'Ref' terminal to be connected, otherwise the value will be 0.
For RGC2/3P..N, the measurement is calculated by accumulating the individual phase power values.

Real Power

The real power reading is recorded in W. This reading is in steps of 1W for RGC1..N and 10W for RGC2/3P..N. This value is updated every half cycle and is a multiplication of the Voltage RMS value and Current RMS value determined in the last half cycle.
For RGC1..N, this reading requires the 'Ref' terminal to be connected, otherwise the value will be 0.
For RGC2/3P..N, the measurement is calculated by accumulating the individual phase power values.

Note that for resistive loads with power factor = 1, the real power and the apparent power will be the same.

Energy

The initial value of this register at power-up is the last reading recording before switch OFF of the NRG controller. In case of a new device this value starts from 0. This reading is the addition of the initial energy value at power-up and the kWh consumed during this power up. This reading is updated in steps of 1 kWh hence a value of 1034 would mean 1034kWh.

SSR Running Hours

This reading records the accumulated time in hours that the output of the RG..N was switched ON. The value is updated every half cycle. The initial reading at power-up is the last reading recorded before switch OFF of the NRG controller. In case of a new device this value starts from 0. This reading is the addition of the initial running-hours value at power-up and the running hours during this power-up. The reading is updated in steps of 1 hour, thus a value of 1034 would mean 1034h that the output was ON during its lifetime. In the event that the counter reaches its maximum value, the counter shall roll back to 0 and start counting up again.

Load Running Hours

This reading records the accumulated time in hours that the output of the RG..N was switched ON. The value of this register is updated every half cycle. The initial value of this register at power-up is the last reading recording before switch OFF of the NRG control. This reading is updated in steps of 1 hour, thus a value of 1034 means 1034h that the output was ON during its lifetime. In case of a new SSR this value starts from 0. This reading can be reset in case of a load or SSR replacement via the Load Running Hours reset setting. A ‘Store Permanently’ command shall be executed after modifying the value.

8. Alarms and Diagnostics

The RG..N and NRGC are equipped with on-board diagnostics to facilitate troubleshooting. The status of the NRGC and the RG..N is readable from the Controller Status Register **CTRSR** and the RG..N End-Device General Status Register **EDGSR** respectively.

The **CTRSR** has a number of flags that identify the specific alarm condition detected. These flags are set when the respective alarm represented by that flag is present in the system. In addition to the raised flag in the **CTRSR**, a visual indication on the NRGC is available through a red LED that switches ON to indicate an alarm presence. A specific flash rate of the red LED helps to identify the alarm type present on the NRGC. The NRGC is also equipped with an auxiliary EMR that changes state whenever an alarm condition is present. This is the default set condition for the auxiliary EMR. This auxiliary EMR may be configured to operate as a general purpose EMR instead of an Alarm EMR or may be configured to operate only for specific alarm types as configured through the Relay Configuration Register **RLYCR**, in which case the operation of the EMR will depend on the configured setting.

The **EDGSR** also includes a number of flags to identify the presence and type of alarm condition detected. Further details on the alarm identified are available through the Alarm 1 Status Register **AL1SR**. Apart from the set flags in the **AL1SR** and **EDGSR**, a visual indication is present on the problematic RG..N through a red LED that switches ON to indicate an alarm presence. A specific flash rate of the red LED helps to identify the alarm type present on the RG..N.

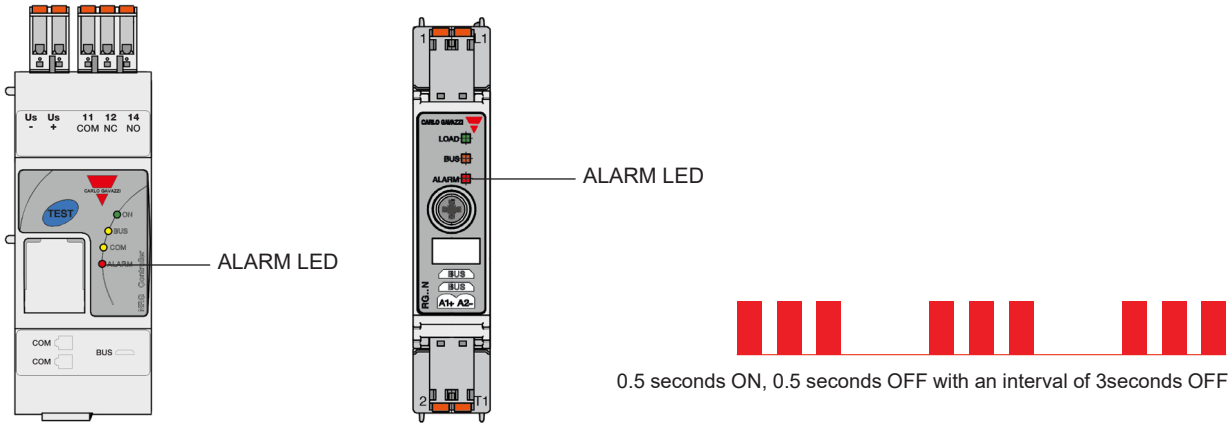


Fig. 12 - Red Alarm LED for NRGC and RG..N and flashing rate

8.1. LED indications - NRG Controller

ON	Green	ON	US is present at terminals Us+, Us-
		OFF	US is not present at terminals Us+, Us-
BUS	Yellow	ON	Transmission of messages from NRGC to RG..Ns
		OFF	Idle bus between the NRGC and RG..Ns or NRGC is receiving data from RG..Ns
COM	Yellow	ON	Transmission of a reply from the NRGC to the main controller
		OFF	Idle bus between the main controller and NRGC or NRGC is receiving data from the main controller
Alarm	Red	2 Flashes	Configuration error *(Device limit error, Device conflict error, Device unconfigured error, Device position error)*
		3 Flashes	Communication (COM) error
		8 Flashes	Communication (BUS) error
		9 Flashes	Internal error
		10 Flashes	Termination error

8.2. LED indications - RG..N

LOAD	Green	ON	SSR output is ON
		OFF	SSR output is OFF
BUS	Yellow	ON	Communication ongoing between NRG controller and RG..Ns
		OFF	Communication between NRG controller and RG..Ns is idle
Alarm	Red	100% ON	SSR over-temperature
		1 Flash	Load deviation
		2 Flashes	Mains loss
		3 Flashes	Load loss / SSR open circuit
		4 Flashes	SSR short circuit
		5 Flashes	Frequency out of range
		6 Flashes	Current out of range
		7 Flashes	Voltage out of range
		8 Flashes	Communication (BUS) error
		9 Flashes	Internal error

8.3. Alarms - NRG Controller

Device Limit Error	
Description	This alarm is issued by the NRGC if after a Sequence Roll Call, the number of RG..Ns detected on the BUS chain is larger than the allowable range; >48 devices for RG..D..N, >32 switched poles for RG..CM..N
Diagnose	Confirm that the number of RG..Ns/switched poles connected to one NRG Controller is within the limit.

Device Mismatch Error	
Description	This alarm is issued if the number of RG..Ns detected on the BUS chain after a Sequence Roll Call or Presence Roll Call or AutoConfig operation does not match the expected number of RG..Ns by the main controller. This alarm is not generated by the NRGC (since the NRGC would not know the user's intended number of RG..Ns to be connected to its BUS chain) but is optionally issued by the main controller through a Set Device Mismatch alarm (refer to Section 6.9).
Diagnose	Confirm that the number of RG..Ns/switched poles connected to the NRG Controller is equal to the set limit.

Device Conflict Error	
Description	Two RG..Ns on the same NRG bus chain have the same address.
Diagnose	Check internal bus connections. If bus connection is correct, do an auto addressing command. Otherwise re-connect the bus as required.

Device Unconfigured Error	
Description	An RG..N on the NRG bus chain does not have an address.
Diagnose	Perform an auto-addressing command.

Device Position Error	
Description	The position of some devices on the internal bus does not correspond to the stored address.
Diagnose	Check alarms on individual RG..Ns on the internal bus for more detail.

Internal Error	
Description	This alarm is issued when a problem arises within the internal circuitry of the NRG controller. In the presence of this alarm, the NRG controller will try as much as possible to proceed with normal operation. It is up to the user to detect the presence of errors reported by the NRGC (through the **CTRSR**) and take action accordingly. When continuing operation with NRGCs reporting an internal error there is a risk that communication may not work correctly or may not be possible, damage may occur to the RG..N devices on the BUS if the internal error is caused by an over-voltage on the supply lines.
Diagnose	Consider replacing the NRG Controller.

Communication (Bus) Error	
Description	This error is issued in case of wrong messages exchanged between the NRG Controller and the RG..Ns.
Diagnose	Not applicable.

Communication (COM) Error	
Description	This error is issued when a consecutive number of wrong messages are received or transmitted or a number of exception errors are sent from the RG..N to the main controller or the NRGC. A count of these wrong messages is kept by category and an alarm is issued if any of the counters reaches the set limit as indicated below. An alarm is issued if either: • 5 consecutive exception response messages are sent to the main controller or the NRGC. Upon sending back a positive reply to the main controller or the NRGC, the exception response messages counter is cleared. • 3 consecutive transmission errors such as: - a message sent back to the main controller or NRGC during which a collision was detected in the transmission The transmissions error counter is cleared when a message is transmitted correctly (without any collisions). • 3 consecutive reception errors such as: - a message is received with byte errors (frame error/parity error/buffer overflow) - a message is received with an incorrect length (either too long >256bytes or too short <4bytes) - a message is received with CRC errors - during message reception bytes are received in between the t1.5 and the t3.5 interframe delay. The successful reception of a message will clear the reception errors counter. The communication error is cleared if none of the above 3 conditions is present.
Diagnose	Not applicable.

Termination Error	
Description	This alarm is issued if the NRG controller detects that the BUS between the NRG controller and the RG..Ns is not correctly terminated. This can be due to: - An internal fault in the NRG controller (start of BUS termination) - RGN-TERMRES is faulty - An internal fault in the RG..N that affects the BUS This alarm (and respective flag **TMERF**) is not cleared until the NRGC is powered-off and powered-on again and the termination of the BUS is found in order. The internal BUS correct termination check is done only at power-up of the NRGC.
Diagnose	Make sure RGN-TERMRES is connected to the last RG..N on the NRG bus chain.

8.4. Alarms - RG..N

In the presence of an alarm condition, all applicable flags in the **EDGSR** and **AL1SR** will be set. The red ALARM LED on the respective RG..N will be ON with a flash rate of the alarm with higher priority.

SSR Over-temperature	
Description	This situation happens when the RG..N does not operate within the rated specifications causing the SSR to overheat. The Temperature Out of Range flag **TOORF** is set and the alarm LED of the RG..N is switched ON (100% ON).The output of the RG..N is switched OFF to prevent the RG..N from getting damaged due to overheating. When the RG..N cools down, the **TOORF** flag is cleared, the Alarm LED is switched OFF, and the RG..N output can be switched accordingly.
Diagnose	Confirm that the RG..N being used is operated within the rated specifications (current rating, spacing and surrounding temperature).

SSR Over-temperature Pre-warning	
Description	This is not an alarm condition and has no effect on the function of the RG..N. The Over-Temperature Pre-warning Flag **OTPWF** is set when the pre-warning margin set on the RG..N is not respected. For example, the **OTPWR** has been set to 40°C and the actual delta is 39°C. In this case, the **OTPWF** would be set. This condition has to be identified by reading the **AL1SR** and it is the user that decides what to do when the **OTPWF** is set. This flag is cleared when the actual temperature reading is ≥ 40°C. The RG..N alarm LED on the RG..N is OFF when the **OTPWF** is set.
Diagnose	Confirm that RG..N used is operated within the rated specifications (current rating, spacing and surrounding temperature.

Load deviation alarm (applicable only for RG..CM..N)	
Description	This alarm works in conjunction with the TEACH Voltage Reference, TEACH Current Reference and TEACH % load deviation settings. If the values of the TEACH Voltage and Current reference are > 0 either through a 'TEACH' command or updated manually; the load deviation alarm is activated. With a TEACH command the values of Vref and Iref registers will be updated by measuring the present current and voltage over a period of time. The TEACH command is refuted in case of alarms present on the system. If the TEACH is unsuccessful, the values of Vref and Iref will be cleared to 0. The TEACH command does not take control of the output of the SSR, it is up to the user to issue a TEACH command when the output is switched ON with a control percentage of > 20% (25% when using Phase Angle switching). The duration of the TEACH procedure shall take up to a maximum of 35s depending on the level of % control. A 'Store Permanently' command is required after a TEACH command for the values of the Vref and Iref to be saved permanently in the device for next power up. The load deviation alarm is issued when a change in resistance > the % load deviation setting is detected. The resistance is measured using the Voltage and Current measurements. The load deviation alarm is useful to detect changes in the load either due to load degradation or partial load failure when more than one load is connected to the SSR. For 3-phase load configurations with RGC2/3P..N, the load deviation of each line is monitored according to the set Vref, Iref and % deviation for each line respectively. If a 1-phase load is connected to the RGC2/3P..N, only the respective lines used for the load configuration will be checked. Unused lines will be ignored. It is important to select the correct load configuration for the RGC2/3P..N via the 'Load Configuration Type' parameter. For RGC2/3P..N, the load deviation alarm is not available with Advanced Full Cycle switching mode.
Diagnose	Check loads for degradation or partial load failure (in case of multiple loads with 1 x RGx1A..N). Take into consideration the load thermal coefficient when setting the percentage deviation in **LDEVPR** to avoid this alarm from being issued unnecessarily.

Mains loss	
Description	Voltage and current signals are missing for more than 3 mains half cycles. The cause is a mains loss. For RGx1..N, the REF terminal must be connected to identify this alarm otherwise the alarm can either be a mains loss or load loss. For RGC2/3P..N, all 3 line-to-line voltages are monitored. The alarm will trigger if the voltage and current signals are missing from any one of the 3 lines.
Diagnose	Ensure mains supply is ON. Confirm that protection (fuses / miniature circuit breakers) have not tripped. Ensure L1 (RGx1..N) or L1 / L2 / L3 (RGC2/3..N) terminals of RG..N are properly connected.

Load loss / SSR Open Circuit	
Description	Load is not switching ON for more than 1 mains half cycle when control signal is present. The cause is either a load loss or an SSR open circuit condition. For 3-phase load configurations with RGC2/3P..N, each line is monitored and if the Load on one of the lines is not switching ON when control signal is present, the alarm will trigger. If a 1-phase load is connected to the RGC2/3P..N, only the respective lines used for the load configuration will be checked. Unused lines will be ignored. It is important to select the correct load configuration for the RGC2/3P..N via the 'Load Configuration Type' parameter.
Diagnose	Make sure that load is not faulty or check that the SSR is in an open circuit condition. If an RG..N is replaced, make sure to follow the re-addressing procedure.

SSR Short Circuit	
Description	This condition is identified when a current >300mA flows through the RG..N output when the control signal is OFF.
Diagnose	Make sure that the appropriate short circuit protection is utilised. If an RG..N is replaced, follow the re-addressing procedure at power-up. Check the load and protection devices (fuses or Miniature Circuit Breakers) status before re-starting.

Frequency out of range	
Description	This condition is identified when the frequency measured by the RG..N (**FQRDR**) is not within the set range, i.e. it is > Over Frequency Limit (**OFLMR**) or < Under Frequency Limit (**UFLMR**). This alarm is issued (**FOORF** is set) if this condition is present for >10 seconds. Though indicated as an alarm condition, this alarm has no effect on the function on the RG..N and it is up to the user to decide what to do when this alarm is activated. The alarm is cleared (**FOORF** cleared and RG..N alarm LED switched OFF) when: **UFLMR** ≤ **FQRDR** ≤ **OFLMR** for >10 seconds.
Diagnose	Check the line frequency and ensure that the over and under frequency limits are set properly. Though the switching function of the RG…N is not affected by this alarm, care must be taken to make sure RG..N is operated within its rated specification.

Voltage out of range	
Description	This condition is identified when the voltage measured by the RG..N (**VRRDR**) is not within the set range, i.e. the measured voltage is > Over Voltage Limit (**OVLMR**) or < Under Voltage Limit (**UVLMR**). This alarm is issued (**VOORF** is set) if this condition is present for >10 seconds. Though indicated as an alarm condition, this alarm has no effect on the function on the RG..N and it is up to the user to decide what to do when this alarm is activated. For RGC2/3P..N all 3 line-to-line voltages are monitored for any voltage fluctuations outside of the set limits.
Diagnose	Check mains and ensure that the over and under voltage limits are set properly. Though the switching function of the RG…N is not affected by this alarm, care must be taken to make sure RG..N is operated within its rated specification.

Current out of range		
Description	This condition is identified when the current measured by the RG..N (**CRRDR**) is not within the set range, i.e. the measured current is > Over Current Limit (**OVLMR**) or < Under Current Limit (**UVLMR**). This alarm is issued if this condition is present for >1 second. Though indicated as an alarm condition, this alarm has no effect on the function on the RG..N and it is up to the user to decide what to do when this alarm is activated (**COORF** is set). The over current limit is bound by the maximum current for each NRG solid state relay variant. A list of the variants with their maximum current values is listed in the table below. The over current limit can be switched off by setting the value to 65535. For 3-phase load configurations with RGC2/3P..N, each line is monitored for any current fluctuations outside of the set limits. If a 1-phase load is connected to the RGC2/3P..N, only the respective lines used for the load configuration will be monitored. Unused lines will be ignored. It is important to select the correct load configuration for the RGC2/3P..N via the 'Load Configuration Type' parameter. For RGC2/3P..N, the current out of range alarm is not available with Advanced Full Cycle switching mode.	
Current limits (RGx1..N)	RGC1x60CM25KEN	3300 (33 A)
	RGC1x60CM32KEN	3300 (33 A)
	RGC1x60CM32GEN	4700 (47 A)
	RGC1x60CM42GEN	6400 (64 A)
	RGC1x60CM62GEN	9300 (93 A)
	RGS1x60CM50KEN	5500 (55 A)
	RGS1x60CM92KEN	9900 (99 A)
	RGS1x60CM92GEN	9900 (99 A)
Current limits (RGC2/3P..N)	RGC2P60CM25KEN	3000 (30 A)
	RGC2P60CM40GEN	4400 (44 A)
	RGC2P60CM75GEN	8200 (82 A)
	RGC3P60CM20KEN	2200 (22 A)
	RGC3P60CM30GEN	3300 (33 A)
	RGC3P60CM65GEN	7300 (73 A)
Diagnose	The over current limit is bound by the maximum current for each NRG solid state relay variant. A list of the variants with their maximum current values is listed in the table above. The over current limit can be switched off by setting the value to 65535.	

Internal error	
Description	This alarm is issued when a problem arises within the internal circuit of the RG..N. In the presence of this alarm, the RG..N will try as much as possible to proceed with normal operation. It is up to the user to detect the presence of errors reported by the RG..N (through the **EDGSR**) and take action accordingly. When continuing operation with RG..Ns reporting an internal error there is a risk that the messages are not correctly received by the RG..N and/or replies will not be correctly received by the NRGC and/or main controller.
Diagnose	Confirm presence of 24V supply voltage on the NRG Controller US terminals. Otherwise, replace the RG..N reporting an internal error.

Communication (BUS) error	
Description	This error is issued when a consecutive number of wrong messages are received or transmitted or a number of exception errors are sent from the RG..N to the main controller or the NRGC. A count of these wrong messages is kept by category and an alarm is issued if any of the counters reaches the set limit as indicated below. An alarm is issued if either: • 5 consecutive exception response messages are sent to the main controller or the NRGC. Upon sending back a positive reply to the main controller or the NRGC, the exception response messages counter is cleared. • 3 consecutive transmission errors such as: - a message sent back to the main controller or NRGC during which a collision was detected in the transmission The transmissions error counter is cleared when a message is transmitted correctly (without any collisions). • 3 consecutive reception errors such as: - a message is received with byte errors (frame error/parity error/buffer overflow) - a message is received with an incorrect length (either too long >256bytes or too short <4bytes) - a message is received with CRC errors - during message reception bytes are received in between the t1.5 and the t3.5 interframe delay. The successful reception of a message will clear the reception errors counter. The communication error is cleared if none of the above 3 conditions is present.
Diagnose	Not applicable

Soft start current limit reached (only available for RGx1/3P..N)	
Description	This alarm works in conjunction with the Soft Start Current limit Register (**SSCLR**). If the current value during soft start is great than the current limit set in **SSCLR**, then a soft start current limit reached alarm will be triggered.
Diagnose	The set current limit may be too low for the nominal current. The recommended current limit value is 1.2 – 1.5 times the nominal current.

Voltage compensation not possible (only available for RGx1/2/3P..N)	
Description	This alarm works in conjunction with the Voltage Compensation Reference Register (**VCREFR**). It is triggered if the mains voltage has deviated too much such that the control level, after the correction factor has been applied, is beyond the control limits (either < 0% or > 100%).
Diagnose	Not applicable

True power compensation not possible (only available for RGx1/2/3P..N)	
Description	This alarm works in conjunction with the True Power Compensation Reference Register (**TPREFR**). It is triggered if the power has deviated too much such that the control level, after the correction factor has been applied, is beyond the control limits (either < 0% or > 100%)
Diagnose	Not applicable

8.5. Troubleshooting of RG..N and NRGC alarms

EDGSR – End-device (RG..N) General Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				VCACTF	RAMPFL	TCHSFLF	TCHBSYF	AL1SF					CMERF	INERF	ACSWSF	DRSTF

AL1SR – Alarm 1 Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						VCNPF	RCLMF	LDF	TOORF	OTPWF	FOORF	COORF	VOORF	EDSCF	SYF2F	SYF1F

RG..N fault condition	Red LED flashes	Registers EDGSR, AL1SR	Cause and Actions	
SSR Over-temperature	ON (100%)	**AL1SF** = 1 **TOORF** = 1	Cause	The temperature exceeds maximum specified ratings and RG..N output is switched OFF irrespective of control signal.
			Recovery	Self-recovery when the temperature cools down. RG..N output switches ON if control signal is present
			Troubleshooting	Confirm that the RG..N used is matched properly to the load connected to it. Ensure proper ventilation in the cabinet and make sure that the RG..N is derated according to the working surrounding temperature
			Recommendations	Ensure that RG..N is operated within rated specifications (current rating and surrounding temperature)
Load deviation (applicable only for RG..CM..N)	1	**AL1SF** = 1 **LDF** = 1	Cause	The current is not within the percentage range set in LDEVPR from reference value LDIREFR. Change in current is not due to change in voltage
			Recovery	Measured current needs to be within the percentage in LDEVPR range from the reference in LDIREFR. The switching function of the RG..CM..N is not affected by the presence of this alarm
			Troubleshooting	Check loads for degradation or partial load failure (in case of multiple loads with 1 x RG..CM..N)
			Recommendations	Though the switching function of the RG..CM..N is not affected by this alarm care must be taken to make sure that the RG..CM..N is operated within its rated specifications. Take into consideration the load thermal coefficient when setting the percentage deviation in LDEVPR to avoid this alarm from being issued unnecessarily
Mains loss	2	**AL1SF** = 1 **SYF1F** = 1	Cause	Current and voltage signals are missing for >3 mains half cycles. (For RGx1..N, REF terminal has to be connected to identify a mains loss alarm otherwise this can be a mains loss or a load loss).
			Recovery	Self-recovery when the fault condition is no longer present.
			Troubleshooting	Ensure the mains supply is ON. Confirm that any protection (fuses / miniature circuit breakers) have not tripped. Ensure L1/L2/L3 terminals of RG..N are properly connected.

RG..N fault condition	Red LED flashes	Registers EDGSR, AL1SR	Cause and Actions	
Load loss / SSR open circuit	3	**AL1SF** = 1 **SYF2F** = 1	Cause	Load is not switching ON for more than a mains half cycle when the control signal is present. The cause is either a load loss or an RG..N open circuit condition.
			Recovery	Self-recovery when the fault condition is no longer present. An RG..N open circuit condition may never recover and may necessitate the problematic end-device to be replaced
			Troubleshooting	Make sure that the load is not faulty or that the SSR is in an open circuit condition. If an RG..N is replaced; procedure at power-up described in Section 6.3 should be followed for configuring a new RG end-device
			Recommendations	If an RG..N is replaced; procedure at power-up described in Section 6.3 should be followed for configuring a new RG end-device
SSR short circuit	4	**AL1SF** = 1 **EDSCF** = 1	Cause	A load current >300mA flowing through the RG..N output without a control signal present.
			Recovery	Self-recovery when the fault condition is no longer present but in this case it's probable that the RG..N will never recover and will need to be replaced.
			Troubleshooting	Check the RG..N outputs (L1-T1 / L2-T2 / L3-T3), if any are shorted then the RG..N has to be replaced.
			Recommendations	Make sure that appropriate short circuit protection is utilised. If an RG..N is replaced; procedure at power-up described in Section 6.3 should be followed for configuring a new end-device. Check load and protection devices (fuses or Miniature Circuit Breakers) status before re-starting.
Frequency out of range	5	**AL1SF** = 1 **FOORF** = 1	Cause	The frequency measured is not within the range specified by the values in the OFLMR and UFLMR.
			Recovery	Condition for recovery: UFLMR ≤ FQRDR ≤ OFLMR. This alarm self recovers when the FQRDR is within the range set by the UFLMR and OFRLM. The switching function of the RG..N is not affected by the presence of this alarm.
			Troubleshooting	Check the line frequency and make sure that UFLMR and OFLMR are properly set.
			Recommendations	Though the switching function of the RG..N is not affected by this alarm care must be taken to make sure that the RG..N is operated within its rated specifications. Allow some margin from the actual frequency to the set values in the limit registers to avoid this alarm from being issued unnecessarily.

RG..N fault condition	Red LED flashes	Registers EDGSR, AL1SR	Cause and Actions	
Current out of range	6	**AL1SF** = 1 **COORF** = 1	Cause	The current measured is not within the range specified by the values in the OCLMR and UCLMR.
			Recovery	Condition for recovery: UCLMR ≤ CRRDR ≤ OCLMR. This alarm self recovers when the CRRDR is within the range set by the UCLMR and OCRLM. This switching function of the RG..N is not affected by the presence of this alarm.
			Troubleshooting	Check the load current and make sure that UCLMR and OCLMR are properly set.
			Recommendations	Though the switching function of the RG..N is not affected by this alarm care must be taken to make sure that the RG..N is operated within its rated specifications. Allow some margin from the actual current to the set values in the limit registers to avoid this alarm from being issued unnecessarily.
Voltage out of range	7		Cause	The voltage measured is not within the range specified by the values in the OVLMR and UVLMR.
			Recovery	Condition for recovery: UVLMR ≤ VRRDR ≤ OVLMR. This alarm self recovers when the VRRDR is within the range set by the UVLMR and OVRLM. This switching function of the RG..N is not affected by the presence of this alarm.
			Troubleshooting	Check the mains voltage and make sure that UVLMR and OVLMR are properly set.
			Recommendations	Though the switching function of the RG..N is not affected by this alarm care must be taken to make sure that the RG..N is operated within its rated specifications. Allow some margin from the actual mains voltage to the set values in the limit registers to avoid this alarm from being issued unnecessarily.
Communication (BUS) error	8	**CMERF** = 1	Cause	This alarm is issued if either: 5x consecutive exception responses are sent to the main controller or NRGC or 3x consecutive transmission errors were detected during transmission or 3x consecutive reception errors were identified in receipt of messages.
			Recovery	This alarm recovers when either a positive reply is sent back to the main controller or the NRGC or a message is transmitted correctly or a message is received correctly.
Soft start current limit reached	-	**AL1SF** = 1 **RCLMFF** = 1	Cause	The set current limit was reached during soft start.
			Recovery	The set current limit may be too low for the nominal current. The recommended current limit value is 1.2 to 1.5 times the nominal current.
Voltage Compensation not possible	-	**AL1SF** = 1 **VCNPF** = 1	Cause	The mains voltage has deviated too much such that the control level after the correction factor has been applied is beyond the control limits (either < 0% or > 100%).
			Recovery	Not applicable.

RG..N fault condition	Red LED flashes	Registers EDGSR, AL1SR	Cause and Actions	
Internal error	9	**INERF** = 1	Cause	Internal issue with the circuitry of the RG..N.
			Recovery	This alarm will self-recover if the alarm condition is no longer present but most probably the RG..N needs to be replaced as alarm won't recover.
			Troubleshooting	Confirm presence of 24V supply voltage on the NRGC Us terminals.
			Recommendations	Replace RG..N reporting an internal error.

CTRSR – NRGC (Controller) Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CTRBF	USBNF							TMERF	DMERF	DLERF	BSERF	CMERF	INERF		CRSTF

NRGC fault condition	Red LED flashes	Register CTRSR	Cause and Actions	
Configuration error	2	**DMERF** = 1	Cause	The number of RG..Ns detected does not match the expected number by the main controller which in turn issues a Set Device Mismatch Alarm command.
			Recovery	After changes to the BUS chain to have the number of RG..Ns as per expectations: • Perform a Sequence or Presence Roll Call or AutoConfig operation without any changes to the BUS chain (i.e., number of RG..Ns do not match expectations by main controller). • Reset the affected NRGC (Note: this will clear the alarm until a new Roll Call or AutoConfig operation is executed. If the result from a Roll Call or AutoConfig operation results in the number of RG..Ns not matching the main controller expectations the alarm is re-issued). • Main controller requests a Clear Device Mismatch Alarm.
			Troubleshooting	The DMERF can be used to highlight this type of error to the machine user on the HMI and give instructions on the steps to be followed to clear this alarm.
Configuration error	2	**DLERF** = 1	Cause	Number of RG..Ns detected on the BUS chain is more than the max. allowed
			Recovery	After changes to the BUS chain to have number of RG..D..N < 48 or number of switched poles of RG.. CM..N < 32: • Perform a Sequence Roll Call without any changes to the BUS chain • Reset the affected NRGC (Note: this will clear the alarm until a Sequence Roll Call operation is executed. If the result of the Sequence Roll Call results in the number of RG..Ns maximum allowed the alarm is re-issued).
			Troubleshooting	Check that the number of RG..Ns connected to the BUS chain is larger than max. allowed depending on the end device model (RG..D..N or RG..CM..N). Check the wiring between NRGC and subsequent RG..Ns

NRGC fault condition	Red LED flashes	Register CTRSR	Cause and Actions	
Communication (COM) error	3	**CMERF** = 1	Cause	This alarm is issued if either: 5x consecutive exception responses are sent to the main controller or 3x consecutive transmission errors were detected during transmission or 3x consecutive reception errors were identified in receipt of messages.
			Recovery	This alarm recovers when either a positive reply is sent back to the main controller or a message is transmitted correctly or a message is received correctly.
Communication (BUS) error	8	**BSERF** = 1	Cause	Not applicable
			Recovery	Not applicable
Internal error	9	**INERF** = 1	Cause	Internal issue with the circuitry of the NRGC.
			Recovery	This alarm will self-recover if the alarm condition is no longer present but most probably the NRGC needs to be replaced.
			Troubleshooting	Confirm presence of 24V supply voltage on the NRGC Us terminals.
			Recommendations	Replace NRGC reporting an internal error.
Termination error	10	**TMERF** = 1	Cause	Termination of the BUS between the NRGC and the RG..Ns is not found in order. This check is done at power up of the NRGC.
			Recovery	Not applicable. Once issued, the NRGC needs to be reset but if the condition is still present, this alarm is reissued.
			Troubleshooting	• Make sure the RGN-TERMRES is connected to the last RG..N on the BUS chain. • Check that no internal errors are reported on any RG..N and NRGC. Replace faulty components. • Check RGN-TERMRES as explained in Section 9.3.1.
			Recommendations	NRGC operation may not be affected with this error however troubleshooting and replacements are suggested to ensure proper system operation.

8.6. Alarm Priorities

In case of multiple alarms occurring simultaneously, the red alarm LED on the NRGC and the RG..N will only show the type of alarm being treated with highest priority. However, the **CTRSR**, the **EDGSR** and the **AL1SR** will have the respective alarm flag, for each type of alarm, set if different alarm types are identified.

9. Service and Maintenance

9.1. Troubleshooting after a Sequence Roll Call operation

Before starting communication with the RG..Ns a Sequence Roll Call operation should ideally be first carried out to ensure that all RG..Ns are correctly configured and are communicating correctly.

Counters **TPRDC** (Total Present Device Counter), **CCFDC** (Correctly Configured Device Counter), **WCFDC** (Wrongly Configured Device Counter) and **UCFDC** (Un-Configured Device Counter) are updated after a Sequence Roll Call operation and their content should be analysed to ensure that everything is in order. It is possible that this is not the case. The table below lists the possible results after a Sequence Roll Call operation:

Case	Result after Sequence Roll Call	Cause	Action
1	CCFDC = TPRDC = Expected no. of RG..Ns WCFDC = 0 UCFDC = 0	n/a – this is the ideal scenario	No further actions needed. The main controller can communicate with RG..Ns
2	UCFDC = TPRDC = Expected no. of RG..Ns WCFDC = 0 CCFDC = 0	1st time power-up (i.e., all RG..Ns are brand new)	AutoConfig is required to configure the RG..Ns
3	TPRDC = Expected no. of RG..Ns CCFDC ≠ TPRDC WCFDC ≠ 0 UCFDC ≠ 0 ≠ TPRDC CCFDC = TPRDC – WCFDC – UCFDC	Un-configured or Wrongly configured RG..Ns due to: • Replacement of a faulty RG..N with a brand new RG..N • Replacement of a faulty RG..N with a used RG..N • Change of physical location (sequence) of a configured RG..N	AutoConfig is required to correctly configure the RG..Ns on the BUS chain
4	TPRDC < Expected no. of RG..Ns TPRDC > 0	• Faulty RG..Ns • RG..Ns removed from the BUS chain	Presence Roll Call, check of wiring, replacement of faulty RG..Ns
5	TPRDC > Expected no. of RG..Ns TPRDC ≤ Max. allowed RG..Ns	More RG..Ns were connected to the BUS chain than intended	Verify that the correct no. of RG..Ns are connected to the BUS chain
6	TPRDC > Max. allowed RG..Ns	More RG..Ns than allowed connected to the BUS chain	Verify that the correct no. of RG..Ns are connected to the BUS chain and remove 'extra' RG..Ns to clear Alarm condition

The above scenarios are explained in further detail below:

Case 2:
UCFDC = TPRDC = Expected no. of RG..Ns
WCFDC = 0
CCFDC = 0

- RG..Ns do not have an alarm status
- **UCFDC** = **TPRDC** = Expected no. of RG..Ns meaning that all RG..Ns are brand new and so need to be configured for the first time
- Perform an AutoConfig operation to correctly configure the RG..Ns on the BUS chain
- Analyse the result of the AutoConfig operation or perform a Sequence Roll Call operation

Case 3:
TPRDC = Expected no. of RG..Ns
CCFDC ≠ TPRDC
WCFDC ≠ 0

UCFDC ≠ 0 ≠ TPRDC (eliminates case 2 scenario)
CCFDC = TPRDC – WCFDC – UCFDC

- RG..Ns do not have an alarm status
- Presence Roll Call is not required since **TPRDC** = Expected no. of RG..Ns
- One or more RG..Ns detected on the BUS chain is/are not correctly configured. They can be:
  - Un-configured:
    - Both RG..N ID and NRGC ID stored in the RG..N = 255, or invalid (0, 49-254).
    - This may happen if a faulty unit is replaced with a brand new (un-used) unit
  - Wrongly configured (RG..N ID and/or NRGC ID do not match the expected values).
    This may happen if RG..Ns were dismantled and re-assembled in the wrong sequence or if a faulty RG..N was replaced with a “used” (not brand new) RG..N that was already configured in the past and has a valid ID but is in the wrong physical location and/or the NRGC ID does not match the ID of the NRGC to which it is connected.

Verification can be done by analysing the contents of the **DCDRxx** (RG..Nxx Configuration Data Register). The **CTCSB** (Controller Configuration Status Bits) and **EDCSB** (RG..N Configuration Status Bits) indicate whether the NRGC ID and RG..N ID read from RG..Nxx are considered Correct, Wrong or Unconfigured. This can be further confirmed by reading the **CNIDRxx** and **EDIDRxx** of the respective RG..N

- It should first be confirmed that the RG..Ns are actually placed in the correct sequence and that the wiring from one RG..N to another in done in a sequential manner.
- If incorrect wiring or wrong RG..N position is identified, this should be rectified.
- Reset the NRGC.
- Perform an AutoConfig operation to correctly configure the RG..Ns on the BUS chain.
- Analyse the result of the AutoConfig operation or perform a Sequence Roll Call operation.

Case 4:
TPRDC < Expected no. of RG..Ns
TPRDC > 0

After a Sequence Roll Call resulting in the **TPRDC** to be less than the expected no. of RG..Ns, the main controller may:

- **Option 1:** Provide an alert on end-machine interface (HMI) for user intervention before proceeding with systems operation.
- **Option 2:** Attempt to proceed with systems operation, if possible, following an analysis of the RG..N Configuration Data Registers **DCDRxx**.

Option 1:
The main controller can alert the machine user to check wiring and ensure that the RG..Ns are not exhibiting any errors on the respective alarm LED. A defective auto-configuration mechanism and/or the communication may result in an internal error (9 flashes of the red LED). In this case, the faulty RG..N(s) should be replaced and the NRGC reset.

Option 2:
Analysis of the RG..N Configuration Data Registers (**DCDRxx**), RG..N ID Register (**EDIDRxx**), and NRGC ID Register (**CNIDRxx**) can result in the following:

1. If the contents of these registers for RG..Nxx are all 0, except for the Configuration Error Flag **CFERF** in **DCDRxx** which can be set or cleared, either RG..Nxx is not present on the BUS, or did not communicate with the NRGC due to a fault. In this case the options are:

   - Stop system operation and alert the end-machine user to check wiring and/or replace a faulty RG..N(s). Reset the NRGC after a replacement.
   - Or, considering that a replacement may not be immediately possible or available: attempt to operate the system despite this fault by requesting a Presence Roll Call operation to check which RG..Ns are present and hence continue machine operation with some missing RG..Ns. The following steps should be followed:
     - Request a Presence Roll Call operation
     - Analyse TPRDC, CCFDC, UCFDC, WCFDC which could give either of the following results:

   i. **TPRDC** = Expected no. of RG..Ns
   In this case all RG..Ns expected to be on the BUS have been detected. The Presence Roll Call

does not utilise the auto-configuration mechanism unlike the Sequence Roll Call and hence the reason for **TPRDC** < Expected no. of RG..Ns after Sequence Roll Call vs. **TPRDC** = Expected no. of RG. Ns after Presence Roll Call is related to an issue with the auto-configuration mechanism. The faulty RG..N with an issue in the auto-configuration mechanism can never be auto-configured or have its alarm cleared unless replaced but can support communication.

ii. **TPRDC** < Expected no. of RG..Ns

In this case the undetected RG..N(s) either have a problem with the auto-configuration mechanism and/or a communications problem and hence cannot be identified. At this point, the main controller has to determine whether to allow system operation to proceed despite the fact that the result of the **TPRDC** is less than the expected no. of RG..Ns. The only accessible RG..Ns will be the RG..Ns that were identified in the Presence Roll Call operation. The case when during the lifetime of the machine, the end user shifts the power load of a faulty RG..N onto another RG..N until a replacement is available would result in a scenario of **TPRDC** <Expected no. of RG..Ns. In the case that the RG..N has a communications problem but can still perform the switching function it may be decided to bypass the faulty RG..N from the BUS so that it does not interfere with the normal operation of the BUS. In the case of a change of wiring it is strongly suggested to reset the NRGC.

2. If the contents of these registers are all as expected ;
   - RG..N ID register **EDIDRxx** matches the physical location (**EDIDRxx** = xx).
   - NRGC ID Register **CNIDRxx** matches the ID of the NRGC to which the RG..N is connected.
   - RG..N and NRGC Configuration Status Bits, **EDCSB** and **CTCSB** respectively in **DCDRxx** are both set to correctly configured.
   - The Configuration Error Flag **CFERF** in **DCDRxx** is clear then there is nothing wrong with this RG..N and the next RG..N can be analysed.

3. If the contents of these registers are all as expected but the Configuration Error Flag **CFERF** is reporting an error, this indicates that most probably there is a problem with the AutoConfig mechanism of that RG..N. If this is the case, the RG..N should be reporting an internal alarm on its alarm LED and additionally, the contents of the **DCDRxx**, **EDIDRxx** and **CNIDRxx** of the next RG..Ns should be all 0s. This should be tackled as indicated in point 1 of Option 2 above.

Case 5:
TPRDC > Expected no. of RG..Ns
TPRDC ≤ Max. allowed RG..Ns

This is the case were the no. of RG..Ns found on the BUS chain is larger than the no. of RG..Ns expected by the main controller. This implies that more RG..Ns than intended were connected to the BUS chain. This condition can only be detected by the main controller.

To facilitate diagnostics, the main controller can request the NRGC to set a Device Mismatch Alarm Error (refer to Section 6.9) that will trigger the red LED on the NRGC with a Configuration Error (2 flashes), will set the **DMERF** in the **CTRSR** and set the auxiliary relay if configured accordingly (refer to **RLYCR** in Section 5.2.1).

Case 6:
TPRDC > Max. allowed RG..Ns

The NRGC can identify a situation where the no. of RG..Ns connected to the NRGC is more than the max. allowed. Unlike case 5, this situation can be detected by the NRGC whereby an alarm LED will be triggered to show a Configuration Error (2 flashes), the **DLERF** will be set and the auxiliary relay will operate if configured accordingly (refer to **RLYCR** in Section 5.2.1).

This condition cannot be detected by a Presence Roll Call operation or an AutoConfig operation.

Apart from the Sequence Roll Call, this situation can also be detected through a Communications Check operation. The RG..Ns that exceed the maximum allowed will not communicate with the NRGC during this check and will have the respective BUS LED OFF indicating no on-going communication.

9.2. Troubleshooting after an AutoConfiguration operation

It is assumed that an AutoConfig operation is requested if after a Sequence Roll Call operation the only remaining issues are related to either un-configured or wrongly configured RG..Ns.

After an AutoConfig operation ,the result from **TPRDC**, **UCFDC**, **WCFDC** and **CCFDC** should be analysed.

If the result is not as expected, a possible reason could be due to one or more RG..Ns refusing to update their ID to the requested one. In this case:

- the particular RG..N should be replaced. Reset the NRGC after replacement.
- if the RG..N(s) cannot be replaced it shall be taken out of the BUS (since it can potentially create collisions with other RG..Ns) and bypassed with the internal BUS cable to the next RG..N and optionally connecting its load to another RG..N. In this case, upon reset of the NRGC, and following a Sequence Roll Call, the TPRDC will be less than the expected no. of RG..Ns. However, if all the remaining RG..Ns are detected, the system may be run as is until the faulty RG..Ns are eventually replaced. This is similar to Case 4, Option 2.1 explained in Section 9.1.

9.3. Troubleshooting NRGC related errors

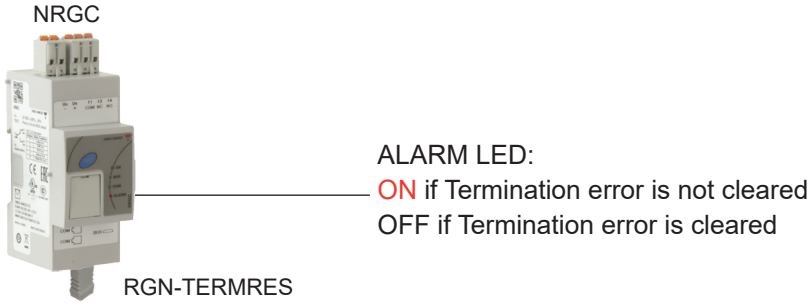
Before commencing operation, the NRGC should be clear of any alarms. The following provides a troubleshooting guide for errors identified by the NRGC.

9.3.1. Troubleshooting a Termination error

This troubleshooting may be required if after verification of the BUS chain wiring and verification that the RGN-TERMRES is mounted on the last RG..N in the BUS chain, the Termination (BUS) error persists.

To find the cause of the Termination error, proceed as follows:

- Power OFF the system.
- Disconnect the BUS chain of RG..Ns from the NRGC. Connect the RGN-TERMRES directly to the NRGC as shown in Figure 13.
- Power ON the system.



If the Termination Error is not cleared, there are 2 possibilities:

- the RGN-TERMRES is faulty
  - replace the RGN-TERMES while the NRGC power is OFF. Upon power UP, if the Termination Error is cleared, then the original RGN-TERMRES was faulty.
- the NRGC has an internal failure
  - if when replacing the RGN-TERMES the Termination Error is NOT cleared, then the cause of the malfunction is probably the NRGC, and may require replacement.

If the Termination error is cleared (ALARM LED OFF):

- the NRGC and RGN-TERMRES are in order
- the error resides in the RG..N(s)
  - check the operation of the RG..N(s) by connecting one device at a time to the BUS chain and connecting the RGN-TERMES to the last device. Power ON the system and check if the alarm is present. The most recently added device that causes the alarm to trigger is faulty and requires replacement.

9.3.2. Verification of the communications line

A Communications Check could reveal certain issues with the communications line during troubleshooting. The Communications Check can be carried out either with the main controller connected to the NRG system but also with the NRGC(s) disconnected from the main controller or PLC. During this check the NRGC attempts to communicate with the RG..Ns on its BUS chain.

Performing a Communications Check without connection to the main controller (PLC)

Apart from troubleshooting, this function is useful to a panel builder who may check the communications line even if the main controller is not available. In this case the front push button 'TEST' on the NRGC shall be used:

- Disconnect the RS485 cable from the NRGC (if connected) after powering off the system.
- Power ON the NRGC.
- Press the TEST push button on the NRGC for more than 2 seconds but less than 5 seconds.

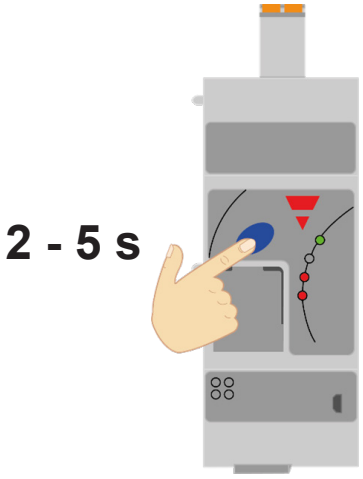


Fig. 13 - Press blue button for 2 - 5s to start / stop the communications check

- If the request is accepted by the NRGC, the Communications Check operation is initiated. The NRGC continuously attempts communication with the RG..Ns present on the BUS (using the auto-configuration mechanism).
- Look visually at the RG..Ns and note that all RG..Ns on the BUS have their BUS LED flashing.
- Check that no errors are reported on the Alarm LED.

Case 1: BUS LED flashing for all RG..Ns, **Alarm LED** is **OFF**
In this case the communications line is functioning well.

Case 2: **BUS LED OFF** for any of the RG..Ns, **Alarm LED** is **OFF**

1. The RG..N(s) with BUS LED OFF may have a fault in the communication system and would need to be replaced.
2. Or the RG..N(s) is connected after a faulty RG..N and could not be reached during the Communications Check operation. In this case, the fault is probably present in the first RG..N that has its BUS LED OFF and/or in the BUS cable connecting the first RG..N that has its BUS LED OFF and/or in the last RG..N that has its BUS LED flashing.
3. Or the RG..N(s) are connected after the maximum number of RG..Ns allowed on the BUS. If more RG..Ns are connected than the allowable range, these are not checked during this operation and will appear as not communicating. The extra RG..Ns need to be removed from the BUS.

Case 3: **BUS LED OFF, Alarm LED ON** (flashing)
This means that the RG..N(s) has either a problem in its auto-configuration mechanism and/or a problem in the communication. The RG..N(s) would need to be replaced. It is very probable that any RG..Ns connected after the RG..N giving an alarm, have their BUS LED OFF because they could not be reached

Power OFF the system or press the 'TEST' front push button between 2 seconds and 5 seconds to terminate the Communications Check operation

Performing a Communications Check through the main controller (PLC)

In this case the main controller is present in the system and is used (possibly through an HMI) to allow a Communications Check Start/Stop operation.

- The main controller requests a command through the **CMMDB** to the NRGC for a Communications Check Start operation.
- If the request is accepted by the NRGC, the Communications Check operation is initiated. The NRGC continuously attempts communication with the RG..Ns present on the BUS (using the auto-configuration mechanism).
- The RG..Ns BUS and Alarm LEDs should be visually checked. Refer to cases 1 to 3 of the previous page.
- Once the Communications Check has been done, the Communications Check operation can be stopped either by the main controller that sends a command through the **CMMDB** to the NRGC for a Communications Check Stop operation or by powering OFF the system.

9.4. Replacing an RG..N

When an RG..N has to be replaced:

1. Connect the new RG..N to the bus chain.
2. Perform an AutoConfiguration procedure (Section 6.5).

Note: RG..N replacements should be performed with the system turned OFF.

9.5. Using the NRG system without ‘REF’ terminal connection

The NRG system can be utilised without connecting the ‘REF’ terminal, however there will be some limitations as listed below:

1. The following readings are not available:
   - RMS Voltage
   - Real Power
   - Apparent Power
2. The ‘TEACH’ operation cannot be executed.
3. The Voltage out of range and Load deviation alarms are not available.
4. The mains loss alarm cannot be discriminated from a load loss. Therefore, a mains loss alarm will indicate either a mains loss or a load loss.

This does not apply for RGC2/3P..N. Voltage reference is not required for these relays.